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Ferroelectric Memory Devices and a Proposed Standardized Test System Design

by

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ABSTRACT

Ferroelectric bulk material devices have been in existence for over 20 years. Not until recently has there been fabrication techniques that consistently and feasibly produce thin film ferroelectric materials. The physical characteristics of thin film ferroelectric capacitors and their subsequent integration into memory design may prove ferroelectric devices to be the ultimate in design for non-volatile, radiation hard computer memory.

This thesis describes current memory systems, some of the recent achievements in ferroelectrics and the prospects for further application of ferroelectrics as an alternative for current memory design. It explores the different testing methodologies being implemented to test ferroelectric devices and suggests a flexible, fully programmable and autonomous new test system design to allow high speed aging and fatigue testing of on-chip ferroelectric capacitors for memory applications.

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I. INTRODUCTION

Thin film ferroelectric capacitors provide the ultimate design for nonvolatile, radiation hard computer memory applications. Designers dream of the ideal nonvolatile memory, which would offer low cost per bit, high density, fast random access, read/write and cycle times of equal duration, low power consumption, operation over a wide temperature range, a single low-voltage power supply, a high degree of radiation tolerance and inherent nonvolatility. Ferroelectric technology is rapidly approaching the "ideal" memory and could become the technology for solid-state disks and electronic image storage, both of which require large amounts of high density, cost effective nonvolatile memory. However, the use of integrated thin film ferroelectric capacitors as nonvolatile memory elements in semiconductor memory design imposes additional electrical performance requirements on the capacitor, therefore it becomes increasingly important during the development of this technology to investigate changes in the electrical behavior of ferroelectric capacitors in a standardized way. Techniques to characterize the fatigue and aging of ferroelectric capacitors for nonvolatile memory applications typically include hysteresis curve measurements because of their intuitive and historical nature, and pulse remanent polarization measurements. Various testing methods

and equipment exist but most are not fully standardized. These differing test procedures can, therefore, lead to inconsistent conclusions. Efforts to develop a standardized testing method have been underway and various companies have designed, built and actively marketed complete testing packages for ferroelectric capacitors. An original Stress Measurement System (SMS) design was developed by Force Technologies and involved using a dedicated 286-16 Mhz Personal Computer (PC). Most recently an equally capable and similar, yet more user friendly design, the RT66A Standardized Ferroelectric Test System was offered by Radiant Technologies. Both systems have inherent limitations and these will be discussed in detail in Chapter III. A proposed new test system design to overcome the limitations mentioned will be developed and subsequent testing and evaluation of this new system design will be examined. Recommendations for possible modifications or improvements will be presented.

II BACKGROUND INFORMATION

To fully appreciate the importance of the integration of thin film ferroelectric capacitors with standard semiconductor memory technology, a review of current memory technology and ferroelectric technology is provided.

A. CURRENT MEMORY TECHNOLOGY

1. Dynamic Random Access Memory (DRAM)

DRAM is the fundamental semiconductor storage cell and consists of a single transistor driver and a storage capacitor. This gives DRAM high density at a low cost but with a complex control circuitry. Information is stored as an electrical charge on a capacitor forming the inter-electrode capacitance of a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). This capacitor is not perfect, it is "leaky," and the charge held on it is gradually lost. Consequently, some mechanism is needed to periodically restore the charge on the capacitor before it leaks away. This process is called "refreshing" and has to be performed at least once every 2 milliseconds. Terminating the refresh cycle due to loss of system power or clock pulse leads to loss of charge on the capacitor and the stored information is lost. Volatility is another difficulty associated with dynamic memory and it is commonly called the alpha particle (helium

ion) problem [Ref. 1]. The capacitance on which each bit of data is stored is exceedingly tiny both electrically and physically. An alpha particle passing through a memory cell can cause sufficient ionization to corrupt the stored data. This condition creates a so-called "soft error," because the cell has not been permanently damaged but has lost its stored data. Careful quality control of the material used to encapsulate the chip can minimize this problem but can never eliminate it. This limits standard DRAM devices that are prone to latch-up and soft errors to applications which do not include high levels of radiation.

2. Static Random Access Memory (SRAM)

SRAM is much easier to use than DRAM. Unlike dynamic memories, static memories do not require periodic refreshing of their contents; nor do they require the address multiplexing circuitry peculiar to DRAM. The basic circuit diagram of a typical N-channel Metal Oxide Semiconductor (NMOS) static storage cell is given in Figure 2.1. The most significant feature of this cell is that six transistors are required to store a single bit of information. Because more components per cell exist in a static memory, a dynamic memory of a given chip size can always store more data (about four times as much) than a corresponding static memory chip of the same size. A close relative of NMOS is Common Metal Oxide Semiconductor (CMOS) logic, which has the highly desirable

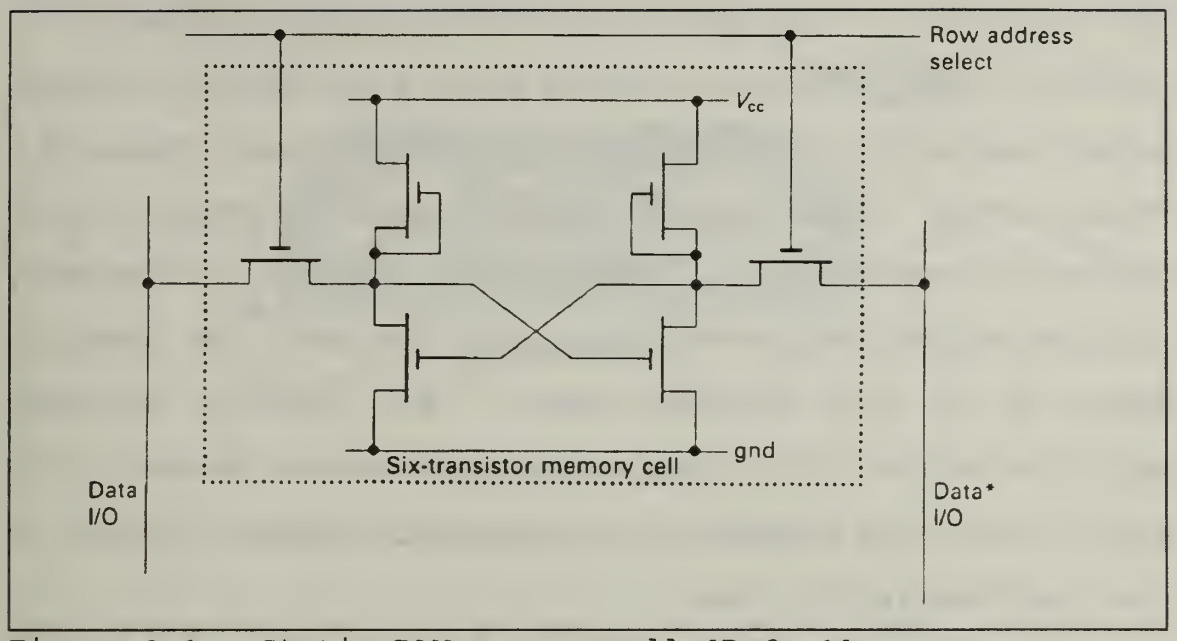


Figure 2.1: Static RAM memory cell [Ref. 1].

property of consuming very little power. A CMOS logic element consumes an appreciable amount of power only when it changes state, so that the power consumption rises with the rate at which a system is clocked. At a sufficiently high clock rate, CMOS systems can consume more power than equivalent NMOS systems. However, when idle, a CMOS component consumes an amazingly tiny amount of power. This allows computers to be designed with nonvolatile memory by powering CMOS chips from small batteries when the system is not connected to the line supply [Ref. 1].

3. Magnetic-core Memory

Using a polarizing material as a magnetic storage medium circumvents both the refresh and volatility limitations of DRAM. Standard design consists of a series of column and

row lines that intersect where the polarizing material is placed. These lines are used to write a "0" or a "1" to the polarizing material at a particular intersection. There is a third set of lines that is used to read an entire row or column of memory cores. Magnetic-core memory is extremely limited by the low integration densities and high specific mass of a unit storage cell. For certain military applications requiring high radiation tolerance however, this over 30 year old technology for nonvolatile memory storage is the most feasible to date.

4. Erasable and Programmable Read-Only Memory (EPROM)

EPROM is a nonvolatile memory component that can be programmed and reprogrammed by the user with relatively low-cost equipment. However, the EPROM must be physically removed from the system board and illuminated by a strong ultraviolet source of light for about 20 minutes prior to reprogramming. This limits their application to terrestrial and non-remote systems. The function of an EPROM is to store programs and data that are never, or only infrequently, modified. An EPROM memory cell consists of a single NMOS field-effect transistor and is illustrated in Figure 2.2. Because the EPROM cell contains a single transistor, densities comparable to DRAM are achieved. The special feature of the EPROM is the "floating gate," which is insulated from any conductor by means of a thin layer of silicon dioxide, an almost perfect insulator.

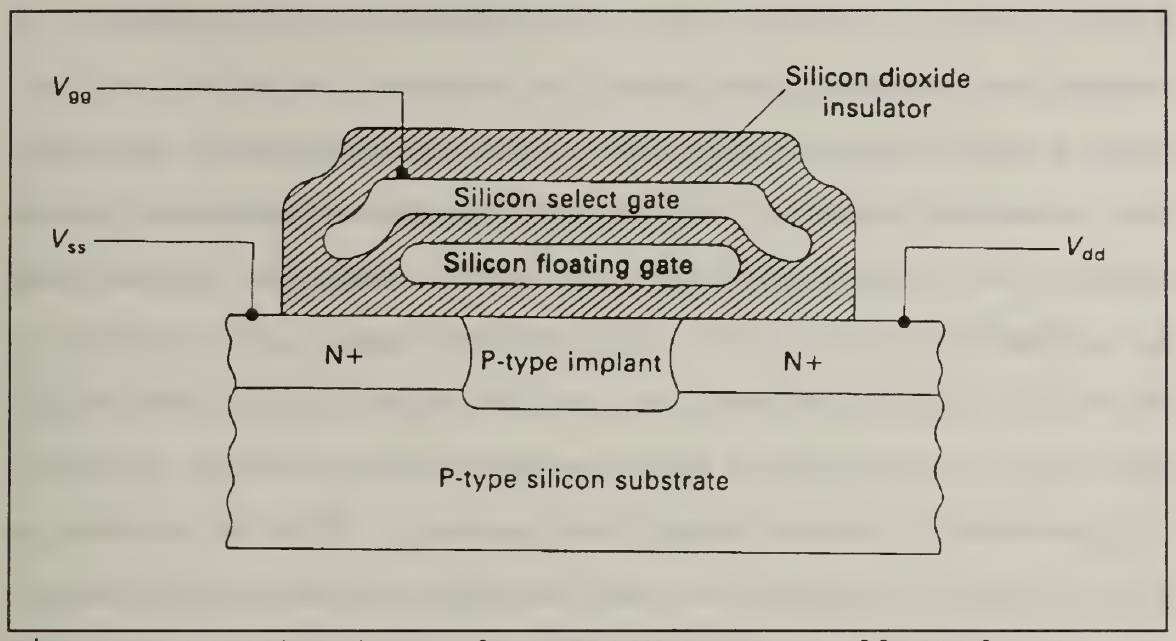


Figure 2.2: Structure of an EPROM memory cell [Ref. 1].

EPROMs are found mainly in four applications: in embedded systems where they hold firmware, in personal computers where they hold the operating system and/or interpreters for high level languages, in bootstrap loaders in general purpose digital systems, and in the development of microprocessor systems. General purpose systems must have at least sufficient EPROM to hold the bootstrap loader that reads the operating system from a disk. Some manufacturers put much of the operating system in EPROM to increase the speed of the system and to reduce the demands on the system read/write memory.

5. Electrically Erasable PROM (EEPROM)

EEPROM cells can be altered with an electric current, typically supplied by an integrated charge pump. EEPROM

technology is limited by the need to perform a bulk erasure of the device in order to change the information in any portion of the memory space. By using two transistors per cell, one for access and one for storage, EEPROMs become architecturally similar to a DRAM except that the DRAM's capacitor is replaced by a floating gate device that stores charge. The charge in that gate can be accessed and can be electrically removed by the access transistor. Since access transistors are used, it is possible to erase data row by row. EEPROMs require a minimum of 12V to write so they are often supplied with an on-board charge pump, requiring only a single 5V external supply. Serial EEPROMs are used as peripheral devices to store user-programmable features for micro-controllers typically equipped with serial interface.

6. Flash Memory

With limited endurance, Flash memories, like EEPROMs, are "read-mostly" devices. Flash is particularly beneficial in cost sensitive applications (like personal computers) where full featured EEPROMs are too expensive. The difference between Flash EPROM and Flash EEPROM has not been settled and users tend to view Flash devices as replacements for either EPROM or EEPROM. All Flash memory can be categorized by "generation." [Ref. 2]

a. First Generation

First generation Flash memory uses dual power supplies (typically 5V/12V), and requires the use of an external sequencer and wave-shaping circuits to implement the programming algorithm. The writing requirements of a first generation Flash are very complex. The designer essentially has to duplicate the specialized sequencers and circuit controls normally found in an EPROM programmer in order to sequence the write voltages and control the write slew rate. It is a complicated algorithm that can consume valuable board real estate and add considerable cost.

b. Second Generation

Second generation Flash memory uses an on-board charge pump to achieve 5V only operation, and contains an on-board sequencer and wave-shaping circuits to make programming easier. The key to second generation Flash is that it has the same system interface as SRAM.

Flash price/density advantages are offset by several disadvantages. One is that all bits must be erased before programming one bit. Further, all bits must be programmed before erasing. Since in many applications program and data are changed in incremental order, when data contained within the Flash is changed, it has to be off-loaded to some other memory location. During this data transfer the data is volatile again. With Flash, there is a trade-off between the

ability to perform a section-only erase versus endurance. If sector erase is needed, endurance drops drastically. Finally, Flash memory is also susceptible to latch-up and catastrophic destruction when exposed to high levels of ionizing radiation.

B. FERROELECTRICS

Ferroelectric technology offers an exciting, new alternative for memory design. This new technology provides nonvolatility, radiation-hardness, low power requirements, increased density and high speed operation. By providing nonvolatility without sacrificing performance, ferroelectric memories could replace several currently used memory devices mentioned previously, thus greatly simplifying computer system architectures.

1. Brief History

Ferroelectric materials are a part of a group of materials made up from dielectric crystals which exhibit unique electrical characteristics. For instance, piezoelectric materials generate electricity or electric polarity when the dielectric crystal is subjected to mechanical stress, and conversely, generates stress in the crystal when subjected to an applied voltage. Pyroelectric materials generate electric charge on the crystal when subjected to a change in temperature. A ferroelectric material is a crystalline dielectric material that can be given a permanent electric polarization by application of an

electric field. The electric polarity remains even after the electric field is removed and it gives the ferroelectric material the unique ability to store binary or even analog data in the state of the material itself.

The study of ferroelectrics began in 1921 when J. Valasek discovered the phenomenon of spontaneous polarization. Spontaneous polarization takes place when the electrical dipoles in the material align themselves along the lines of an electric field applied to the specimen and remain aligned even after the field is removed. Reversing the electric field then causes the alignment of the electric dipoles to switch polarity. Valasek applied an electric field across a Rochelle Salt sample ($NaKC_4H_4O_6 4H_2O$) and even though there was no iron in the substance, the similarity between the non-linear hysteretic dielectric properties of Rochelle Salt and the magnetic behavior of ferromagnetic iron was so similar, it prompted Valasek to call the material ferroelectric. In 1935, G. Busch and P. Scherrer discovered the piezoelectric properties of Potassium Dihydrogen Phosphate (KDP) and two years later A. Keller, utilizing KDP, developed the first piezoelectric transducer. In 1940, Barium Titanate ($BaTiO_3$) was simultaneously discovered by several groups throughout the world to have ferroelectric properties. From 1950 to 1960, 20 new materials that exhibited ferroelectric characteristics were discovered. In the 1960's, IBM studied thick-film or

bulk ferroelectric technology as an alternative to magnetic core memory technology but finally terminated research in 1973 primarily due to the following reasons [Ref. 3]:

1. Ferroelectric memories could not be addressed by a combination of voltages on the row and column lines the way a ferromagnetic memory could.
2. After a finite number of read/write cycles, the materials exhibited fatigue and retention problems.
3. They lacked a deposition technique that could consistently achieve high quality submicron films.
4. Because bulk materials were used, the devices required very high operating voltages (in excess of 40V) in order to achieve the required electric field to achieve a polarization reversal.

In the past 20 years much progress has been made in the fabrication of thin-film ferroelectric materials. It is the thin-film quality which has made possible the compatibility and integration with existing semiconductor technology. Most of the memory devices under development are based on conventional CMOS circuitry and are completely compatible with existing designs and fabrication procedures. Several companies are currently involved (McDonnell-Douglas, Raytheon, Westinghouse, Radiant, National Semiconductor, Ramtron, TRW, Polaroid, Texas Instruments and Symetrix to name a few) in developing memories based on ferroelectric materials. Ferroelectrics have already proven to be practical in other areas, such as piezoelectric transducers, pyroelectric detectors, and electro-optics. The potential of

ferroelectrics for applications in nonvolatile semiconductor memory is the motivation behind developing thin-film ferroelectric memory technology.

2. Physical Characteristics

All dielectric materials exhibit a polarization or charge per unit area on the surface when an external electric field is applied. When the electric field is removed, the polarization disappears, unless it was permanent or "spontaneous electric polarization." If the dielectric material has a crystal structure that lacks a center of symmetry, it can exhibit piezoelectric qualities; that is, application of mechanical stress will induce an electric charge and inversely, application of an electric field will produce proportional strain. A small number of piezoelectric materials have a unique polar axis in the unstrained condition. The unit cells are aligned such that the dipole moments produce a finite and permanent polarization. Pyroelectricity is when the resultant dipole moment changes in magnitude when the material is uniformly heated or cooled, generating an electric charge at the surface of the material as the polarization changes. All ferroelectric materials exhibit both piezoelectric and pyroelectric qualities, but ferroelectrics are unique in that the spontaneous polarization can be reversed with the application of an external electric field [Ref. 4].

a. Crystal Structure

The primary ferroelectric compound of interest is currently Lead Zirconate Titanate (PZT), a ceramic material in the perovskite crystal family. Actually PZT is a continuum of materials with the formula $PbZr_xTi_{1-x}O_3$ where x varies between 0 and 1 [Ref. 5]. PZT is often described by its Zr/Ti ratio. For example if $x=.6$ one would say 60/40 PZT.

The general chemical formula for the unit crystalline cell of a perovskite is ABO_3 and its crystalline

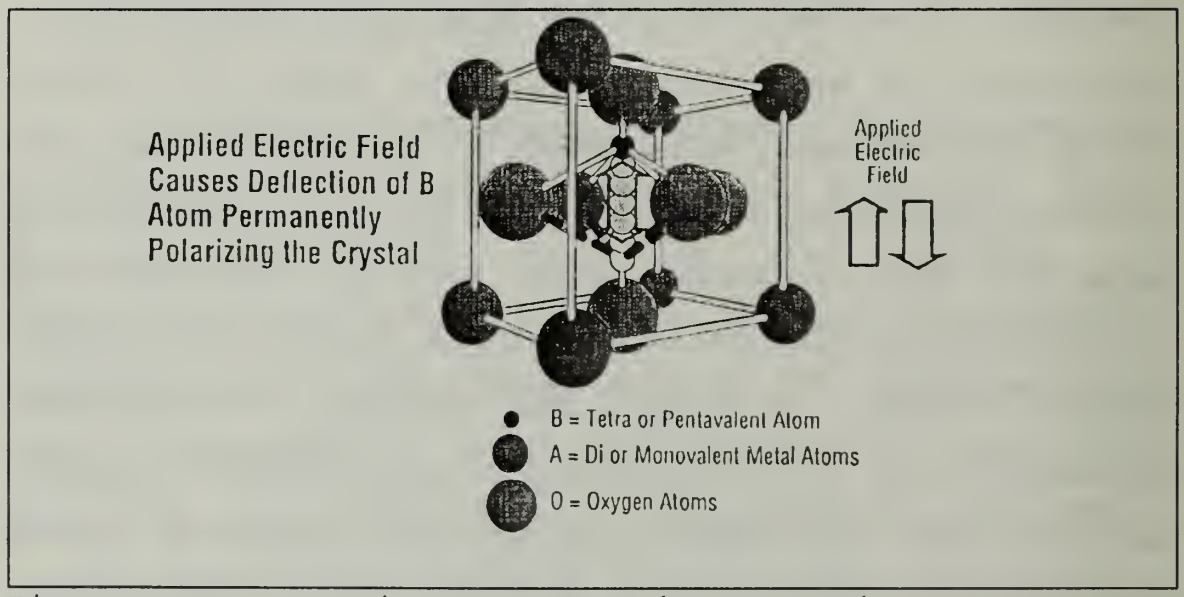


Figure 2.3: Generic Ferroelectric Perovskite Crystal type ABO_3 [Ref. 10]

structure is shown in Figure 2.3. "A" is a metal cation, usually with a valence state of +2, +1 or +3. "B" is a metal cation with a valence state of +4, +5 or +3. "O" is oxygen with a valence state of -2. As the figure depicts, the A

cation at the corners of the unit cell have a large radius while the B cation is relatively small. The oxygen atoms positioned at the face centers have the largest atomic radius. The materials of interest for ferroelectric memory applications have a tetragonal, polar structure. A cubic, unit cell is stretched along one axis and shrunk along the two others by the electric polarizing field. The horizontal, longer axis is referred to as the "a" axis and the shorter, vertical are the "c" axes. The asymmetric position of the B ion, resulting from a difference between the center of positive and the center of negative charge, gives the unit cell its electric dipole. The external charge per surface area ($\mu C/cm^2$) or polarization resulting from this dipole can then be measured. This polarization is permanent due to the attractive-repulsive forces in the unit cell until an external electric field moves the B ion from its position. Ferroelectric materials are then characteristically formed from ions with certain valence relations and atomic size ratios [Ref. 6].

b. Temperature and Poling

The switchability of polarization implies that the energy between directional states is very low. It further implies that the non-polar state is only slightly less stable, so increasing the temperature will cause the material to become nonpolar [Ref. 7]. Ferroelectric materials have a

particular transformation temperature at which they become non-polar and therefore exhibit no spontaneous polarization. This transformation temperature is the Curie point (T_c) and above this temperature (approximately 360°C for PZT) the material is said to be in paraelectric phase. In the paraelectric phase, the dielectric permittivity (ϵ) follows Curie-Weiss behavior in that ϵ is inversely proportional to the difference between the temperature of the material (T) and T_c

$$\varepsilon = \frac{C}{T-T_c} \qquad (1)$$

where C is the Curie constant (°K). As a sample of ferroelectric material is cooled through the curie temperature from a paraelectric state to a ferroelectric state, the crystal lattice becomes asymmetric or polar. The polar structure then displaces the ionic and electronic charges within the unit cell, resulting in a microscopic electric dipole moment. The cells that align with neighboring cells in a common orientation are said to be in the same domain. When several domains are randomly polarized in a material the net macroscopic result is no or very little net polarization. To achieve common orientation within domains, the ferroelectric material is "poled". Poling is the application of a dc electric field to reorient the polar axis of the domains in a

common direction [Ref. 8, p. 3]. The electric field required to reorient the domains is a minimum at T_c so poling is done as the material is cooled through T_c. For memory design and especially for military applications when specifications require operation at 125°C, it is important to know that several properties are affected by temperature. The remanent polarization decreases with increasing temperature and this leads to faster switching speeds. Unfortunately, the aging and fatigue of the cell is also accelerated at temperatures above 85°C [Ref. 4]. Therefore only materials with T_c significantly above 125°C should be used in military applications.

c. Polarization

When the electric field is removed the material will retain a net polarization or remanent polarization (P_r). When an electric field or voltage is applied in the opposite direction, the polarization will "switch" directions to the opposite sign. The net result of a volume of charge dipoles normal to the surface of a thin film of material will appear as though a sheet of equal and opposite charge is bound on the two surfaces of the film. With a suitable conductive electrode material in contact with the surfaces to supply mobile compensating charge, the macroscopic result is a classical parallel plate capacitor which has the unusual ability to store charge. A common way to quantify this

behavior is through the distinctive hysteresis loop of ferroelectric materials as shown in Figure 2.4.

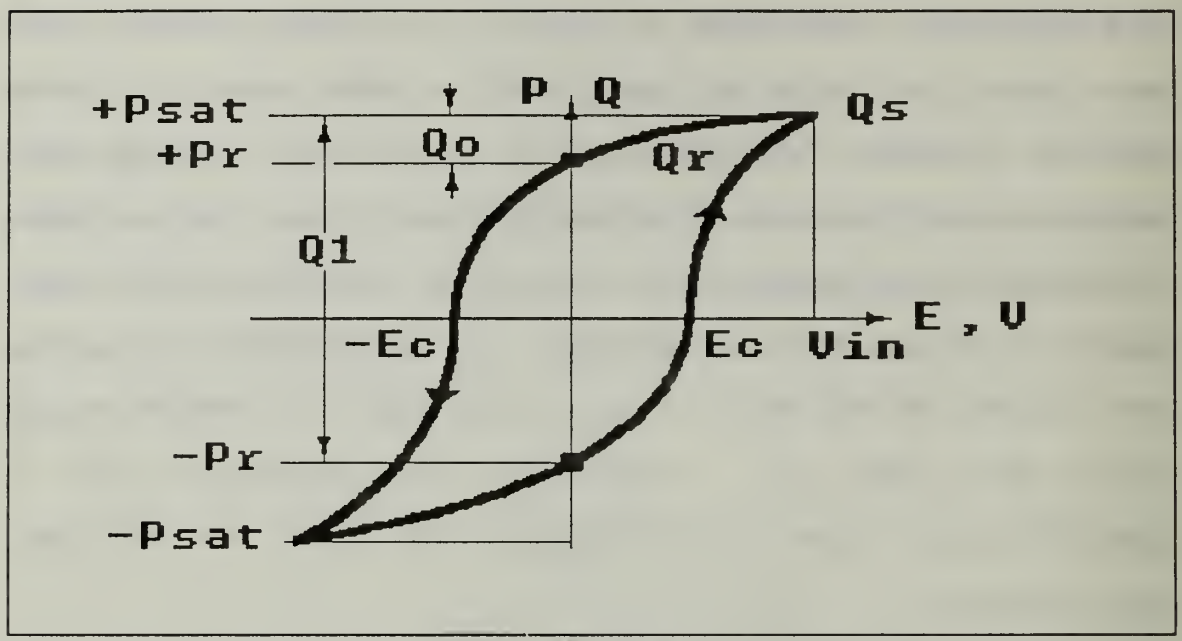


Figure 2.4: Characteristic hysteresis curve of a Thin-film Ferroelectric Capacitor. Polarity versus Electric Field.

To a scientist, this curve represents the Polarization versus Electric field relationship while to the engineer, it represents the Charge versus Voltage relationship. For a conventional linear (sense) capacitor, the charge versus voltage relationship is a straight line with a constant slope C=Q/V. Applying a sufficiently large positive electric field or voltage to a ferroelectric capacitor drives the hysteresis curve into positive saturation, P_{sat} or Q_s. When the voltage is removed the capacitor relaxes to its remanent state, representing a digitally stored "0" (see Figure 2.5). This sequence represents the writing of a "0" into the memory element. Similarly, with a negative voltage, the capacitor is

charged to its negative state representing a stored "1". To read out the contents of this memory element, a positive voltage V_{in} is applied to the ferroelectric capacitor. If the element was in the "0" state, a small charge Q_o will be liberated. If the element was in the "1" state, a much larger Q_1 will be liberated. We measure this liberated charge through the use of the Sawyer-Tower circuit depicted in Figure 2.5.

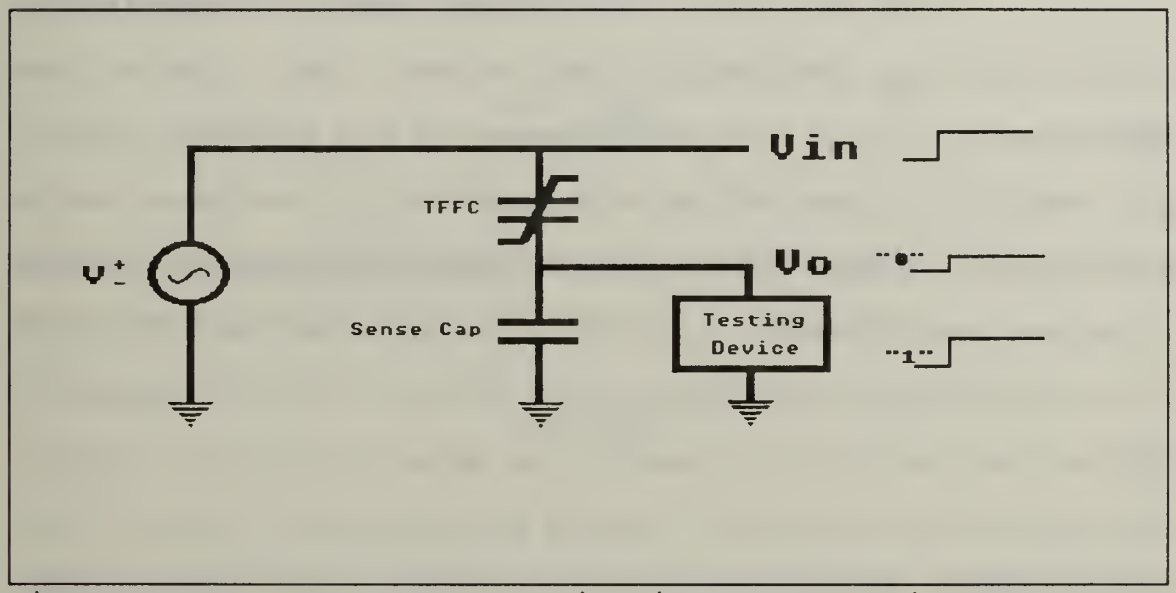


Figure 2.5: Sawyer-Tower Circuit and associated readout waveforms [Ref. 3]

In this circuit, the charge flows into the much larger linear sense capacitor (capacitance C_s) which develops an output voltage V_o directly proportional to Q by the relation $V_o=Q/C_s$ [Ref. 5]. We observe the hysteresis curve directly by using the Sawyer-Tower circuit and an x-y oscilloscope, with the x-

axis driven by the input voltage and the y-axis by the output voltage. The polarization P, measured in $\mu C/cm^2$, is calculated from $P=Q/A$, where A is the electroded surface area of the ferroelectric film. The electric field, E measured in Volts/cm, is calculated from $E=V/d$ where d is the distance between top and bottom electrodes or the thickness of the sample [Ref. 11: p. 3].

d. Switched Charge

The "switched charge" or charge in motion is current and by integrating the current over time we can associate a voltage with the movement of the switched charge. The common polarization value for determining how much charge will result from a ferroelectric capacitor when it changes polarization is about 20 $\mu C/cm^2$ [Ref. 9]. The coercive field E_c, is the minimum magnitude of the electric field required to ensure that the polarization of the material reverses itself. The switching time can be reduced by applying a larger field. The circuitry used and the size of the cell also influence the switching speed, with smaller size and lower load resistances decreasing switching time [Ref. 4]. In ferroelectric capacitors, not all the grains will switch orientation at the same time. The process is not instantaneous and varies proportionally with film thickness. For 4000 angstrom films it lasts about 10 nanoseconds [Ref. 9]. As the capacitor changes its polarization in the presence of an external

electric field, charges are set in motion due to the change in electrical equilibrium at the surface of the capacitor. The basic relationship between the ferroelectric dielectric constant κ ($\kappa \approx 10^4$), and the polarization P is

$$\kappa = \frac{P}{\varepsilon_o E} \tag{2}$$

where ϵ_o is the permittivity of free space, and E is the field used to produce the polarization [Ref. 3]. The equation for capacitance of a ferroelectric is

$$C = \frac{\kappa \varepsilon_o A}{d} \tag{3}$$

Substituting κ from equation (2) into equation (3) yields capacitance C=AP/V. For current in a capacitor

$$i = C \frac{dv}{dt} \tag{4}$$

Substituting for C, multiplying both sides by dt, assuming the voltage is constant and integrating yields

$$\int i \, dt = \int \frac{AP}{V} \, dV \tag{5}$$

Solving equation (5) and dividing both sides by t yields

$$i = \frac{AP}{t} \ln(V) \tag{6}$$

For the unswitched case, $P=P_{sat}-P_r$. For the switched case, $P=P_{sat}-(-P_r)=P_{sat}+P_r$. This clearly shows that the magnitude of *i* is greater for the switched case. Assuming *V* is constant, it appears that the current is infinite when *t* is very small. In fact voltage is not constant. Therefore, at the beginning of the pulse when *t* is very small, *ln(v)* is the dominant part of the equation, preventing infinite current. After that, *1/t* is the dominant part of equation (6) and the classic current versus time response depicted in Figure 2.6 is the result.

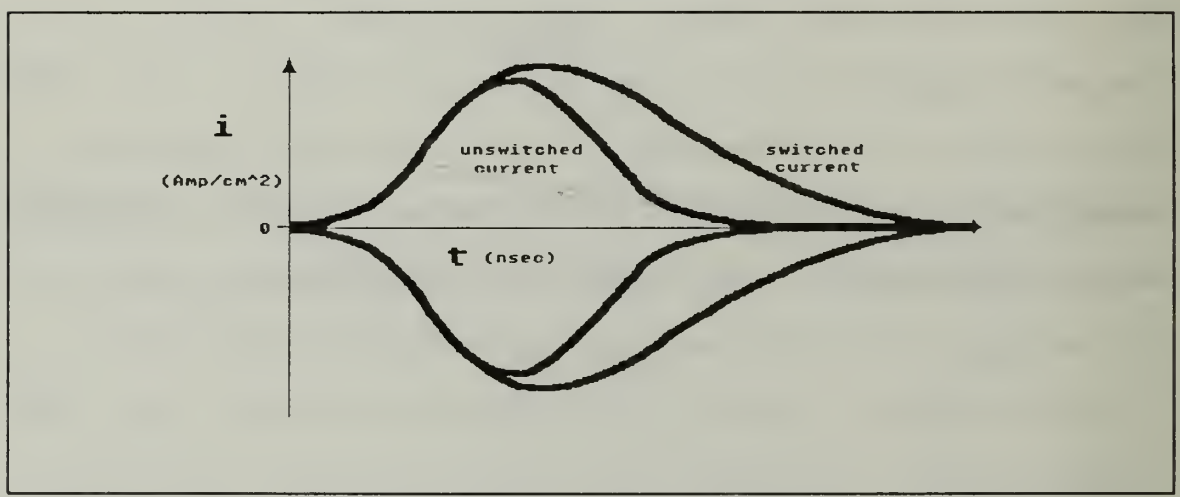


Figure 2.6: Current versus Time response of ferroelectric materials

Integrating the switched and non-switched current curves and getting the difference gives the area between the curves.

$$Q_s = \int (i_{switched} - i_{non\text{-}switched})\, dt \qquad (7)$$

This is the total switched charge.

In summary, "writing" to the ferroelectric capacitor by applying an appropriate electric field causes a polarity corresponding to a "0" or "1". To "read", simply apply another electric field, namely a pulse. The "read" operation basically involves detecting the difference between the two output current signals. If the dipoles are in the direction of the applied field, a current pulse corresponding to the charging element of the capacitor is generated. This current can be considered proportional to the linear dielectric of the ferroelectric capacitor. If the dipoles are oriented in the opposite direction, a larger current pulse forms consisting of capacitor charging current and the switching current caused by the switch in polarity of the dipoles. Since the polarity is now different than what was written, this is considered a destructive read-out (DRO) operation. The data then has to be rewritten following all "read" operations and this can add to fatigue. Using a non-destructive read-out (NDRO) operation would no doubt reduce fatigue. Recently, Radiant Technologies engineers have fabricated and tested a ferroelectric NDRO device [Ref. 13].

e. Dielectric Permittivity

Ferroelectric materials posses unusually high values for dielectric permittivity ($\epsilon > 100$); much higher than the 1-10 range for nonpolar dielectrics [Ref. 11: p.360]. Integration of high permittivity dielectric thin films onto

insulators and semiconductors by chemical processing has led to an understanding of interfacial effects and their influence on electrical and optical properties. In ferroelectric materials, ϵ is not a dielectric "constant" since it varies with electric field and temperature. It is a non-linear function of the electric field and is nearly proportional to the slope of the hysteresis curve [Ref. 12: p.19]. It is also different for each axis of the basic crystal structure [Ref. 11: p.36]. It is a function of material composition and structure, frequency of the applied electric field and time. For memory applications, the ferroelectric film must have a dielectric permittivity that is relatively stable over a wide range of temperatures and ultra high speed switching (f > 1 MHz) for minimal fatigue [Ref. 4].

f. Film Thickness

As mentioned earlier, film thickness and size affects switching speed. It also affects ϵ, P_r and E_c. Recalling the Sawyer-Tower in Figure 2.5 and reviewing the polarization versus area (A) and electric field versus thickness (d) relationships

$$P = \frac{(V_o\ C_{sense})}{A}, \qquad E = \frac{(V_{in} - V_o)}{d} \tag{8}$$

it is simple to see their effect. For fast operation speeds you need thinner films, but as you reduce the film thickness,

E_c increases. The dependencies of E_c and switching speed on film thickness support theories of three-dimensional domain switching, where the lateral domain wall velocities are the rate-limiting factor in polarization switching [Ref. 4].

g. Radiation Effects

Although E_c and P_r can be affected by high doses of radiation, ferroelectric materials are still extremely tolerant to radiation exposure. Low doses of radiation (less than 10^{13} neutrons/cm^2) have an insignificant effect on the ability of the material to maintain its polarization and to switch charge [Ref. 7: p. 90, Ref. 4].

Ferroelectric devices made from PZT can be fabricated that can survive radiation exposures well in excess of 10 Mrad(Si). In addition, radiation induced degradation is recoverable by a postirradiation biased anneal and can be prevented entirely if devices are cycled during irradiation [Ref. 17]. Sandia National Laboratories irradiated 50/50 PZT Krysalis and 65/35 PZT National Semiconductor thin-film ferroelectric capacitors using 10 keV x-ray and 1.1 MeV Co-60 sources to dose levels up to 16 Mrad(Si). Harry Diamond Laboratories tested Arizona State University 52/48 PZT using 10 keV x-rays to dose levels up to 100 Mrad(Si). Radiation induced degradation was observed in all samples mentioned and they appear to be a result of charge transport and trapping in the ferroelectric material or ferroelectric-electrode

interface, altering the local polarizing field and therefore the switching characteristics of the ferroelectric. Significant hysteresis loop distortion, based on radiation-induced grain boundary charging of grain boundaries and interfaces, can be observed at doses greater than five Mrad(Si). The nature of the observed hysteresis loop distortion and the magnitude of polarization loss depend on the polarization state and the applied bias during irradiation. Remanent polarization ($2 \cdot P_r$) however can be restored simply by cycling the ferroelectric capacitor after exposure to radiation. Biasing the ferroelectric capacitor while it is cycled involves placing a voltage, other than common ground, on the ferroelectric-sense capacitor junction in the Sawyer-Tower test configuration. During incremental radiation and post-radiation, the difference between the polarizations ($+P_r$ and $-P_r$), when the sample is switched positive and the bias is removed and when the sample is switched negative and the bias is removed, can be extracted from the hysteresis curve. Unbiased samples (see Figure 2.7) show a larger recovery by cycling than do the samples irradiated with static or dynamic bias (see Figure 2.8). The amount of degradation, however, was larger for the unbiased samples. A distortion and decrease in $2 \cdot P_r$ develops with increasing radiation dose, but the distortion is removed with

post-radiation cycling along with a partial recovery of $2 \cdot P_r$ [Ref. 18].

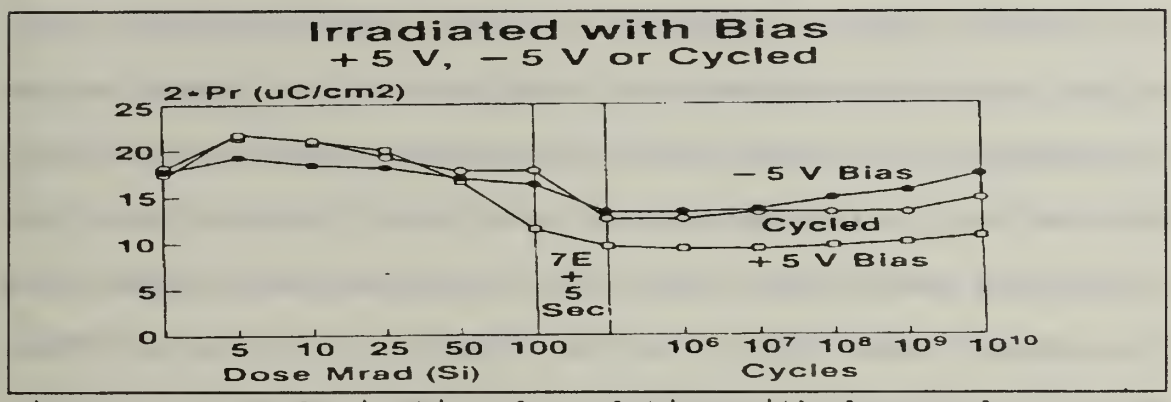


Figure 2.7: Polarization degradation with dose and recovery with cycling for samples irradiated with bias. There was a 7×10^5 sec. delay between the last dose and the first cycling test [Ref. 18].

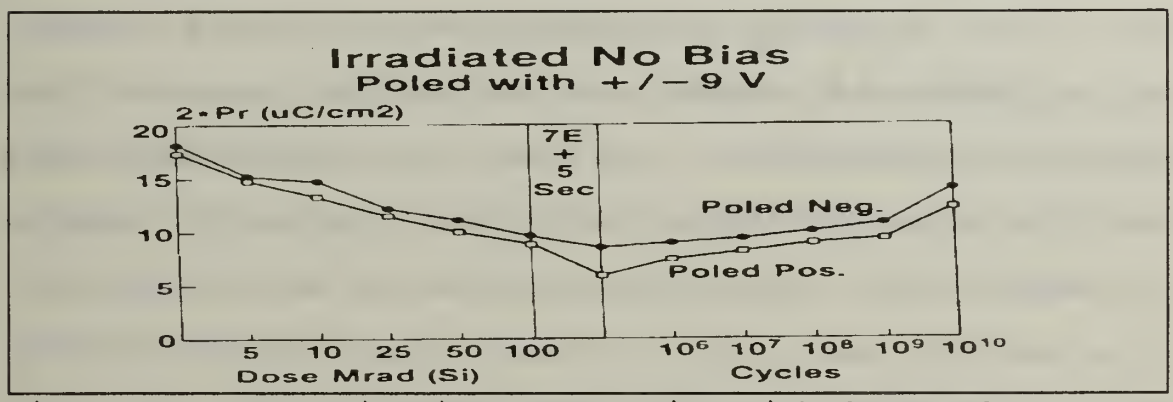


Figure 2.8: Polarization degradation with dose and recovery with cycling for samples irradiated with no bias [Ref. 18].

Standardized testing methods still need to be developed and more work is needed on similar PZT samples and other ferroelectric films to further understand the effects of ionizing radiation on the ferroelectric material and their electrode interface effect.

h. Grain Size

Ferroelectric material grain size has a significant effect on E_c, T_c, P_r, polarization switching time, aging rate and resistance to fatigue. E_c, T_c, polarization switching time, aging rate and fatigue rate are inversely related to grain size while P_r is directly related [Ref. 4]. Grain size becomes important when considering which deposition technique to use. Each produces a certain size and with this comes a certain performance.

3. Degradation Mechanisms

a. Aging

Aging can be defined as the loss of remanent polarization that occurs with no external electric field applied to the material. For memory applications this means the time dependent degradation without experiencing reads or writes [Ref. 4]. Retention refers to the maximum amount of time that the memory can go without a refresh cycle [Ref. 3].

The mechanisms of aging are not yet fully understood. It is known that aging decreases ϵ, P_r, E_c and maybe even P_{sat}. The hysteresis loop changes shape and shifts along the abscissa due to the degraded polarization. Also the aging effects are not exponential but linear with the logarithm of time. It is generally accepted that aging is a result of stabilization of the domain pattern in the ferroelectric material [Ref. 4].

One theory links aging with the degree of tetragonality in the sample crystal structure [Ref. 22: p.5]. The domain structure tends to relax to a more stable, low stress condition. Recall that most ferroelectrics are cubic in the paraelectric state and tetragonal in the ferroelectric state, when poled below the curie temperature. As the unit cell stretches from the cubic to the tetragonal structure, internal strain is created and the nucleating domains are randomly oriented. Over time the domain structure will move toward a more stable state causing the material characteristics to change. For tetragonal structures, this results in domains oriented with lattice axes 90° apart. As the domains reorient they become trapped or "clamped" in the new configuration so the ability to switch polarization is reduced. The rate of aging tends to decrease with increasing tetragonality and also as the material is heated toward its transition phase.

Another theory for aging is the dependency on the distribution and mobility of space charge in the material [Ref. 21 p. 1236]. The space charge is ionic and may result from dopants, impurities or vacancies. The space charge tends to counteract the polarization generated by an external electric field. Consequently, to reverse the polarization the electric field must be large enough to overcome the space charge field. This forces the electric field to no longer be the same in magnitude in both directions and the hysteresis

loop is shifted horizontally along the E axis. This can lead to "read" errors since the charge differential has been reduced for the storage of either a "1" or a "0". The switching time becomes faster when the applied electric field is in the same direction as the space charge field. Also, the larger the resistivity of the material, the more slowly the space charge relaxes [Ref. 21: p. 1243]. Donor doping increases the resistivity and therefore doping PZT with donor impurities tends to lower the aging rate [Ref. 22: p. 22].

The aged material however can be restored to its original condition by heating it above its curie temperature. Also, applying strong alternating current (ac) fields for up to 10^5 cycles will de-age the material [Ref.4].

b. Fatigue

Fatigue can be defined as the loss of remanent polarization that occurs when the material is subjected to an external electric field which either switches the polarization state or reinforces the existing state by driving the polarization from $\pm P_r$ to $\pm P_{sat}$. Fatigue is a function of the number of polarization reversals. Therefore, in memory applications it is dependent on the number of read-write cycles the ferroelectric capacitor has experienced [Ref. 4]. Endurance refers to the total number of read-write cycles the ferroelectric capacitor can endure before failure as a memory device [Ref. 3].

Similar to aging, the mechanisms of fatigue are not yet fully understood. As a sample fatigues, P_r, P_{sat}, and switching time decreases while E_c increases. The hysteresis loop becomes less square and microcracks or dendritic growths may appear [Ref. 23: p. 1550, Ref. 24: p. 100]. The rate of fatigue is a function of the material and for materials being considered for memory applications, the point of failure is on the order of 10^9 to 10^{12} cycles [Ref. 4]. Memory cell design can also affect fatigue rate, especially when it involves DRO versus NDRO. The fatigue can be seen after a characteristic number of cycles and continues with the logarithm of cycles.

One theory for fatigue involves the growth of microcracks witnessed when the material is cycled enough times [Ref. 23: p. 100]. Microcracking is an inherent effect of the mechanical coupling of the piezoelectric materials and the increase in coercive field could be due to the impact of microcracks near the electrode [Ref. 23: p. 97]. Cycling with high electric field strengths speeds up fatigue, changing fatigue limits by as much as a factor of 10^6. This is why it is important to specify the cycling field along with other parameters affecting fatigue. It is possible however to "de-fatigue" the material by heating or cycling at high temperature without trying to alter the microcracks [Ref. 4].

Another theory for fatigue involves the electro-migration of ions and charge defects or the pinning of domain

walls [Ref. 24: p. 1547]. There is a Russian theory of mobile ion diffusion causing an accumulation of space charge along domain walls. This implies an activation energy typical of ion hopping in a polar crystal [Ref. 4]. Fatigue was observed to be reduced at higher temperatures and the degradation or change in switched charge could be described by the following relationship:

$$\frac{dQ}{dn} = A \cdot e^{\left(\frac{-b}{kT}\right)} \tag{9}$$

where Q is the switched charge, n is the number of cycles, T is the temperature in °K, k is Boltzmann's constant (1.381×10^{-23} J/°K) and b is an activation energy of 0.7 eV.

Another theory for fatigue put forth by a group of Americans involves dendritic growth caused by oxygen deficient filaments growing from the interface between electrode and the ferroelectric material [Ref. 3]. Mobile oxygen ions are believed to be freed by the fatigue process by the degradation of a unit cell. These ions then move through the lattice structure until they reach the top or bottom of the material. This is where the dendrite begins to form and more and more mobile ions build on this growth until both top and bottom of the material are joined by this growth. When this occurs, the material shorts and begins to conduct. This accounts for the

faster switching time (higher electric field experienced in the material).

A related theory concerning fatigue involves mobile ions (oxygen, impurities and dopants) [Ref. 25: p. 1400]. These mobile ions contribute to fatigue by collecting at grain boundaries and other defect sites, effectively pinning the domains and restricting polarization reversals through buildup of space charges.

c. Waiting Time

Waiting time can be defined as the spontaneous reorientation of the material to a preferred state. It is the inclination of some materials to switch back to a preferred state, following domain reorientation due to an external electric field [Ref. 4]. The result of waiting time effect is an asymmetry in the switched polarization, which is dependent on the length of time the cell has been held in either the $+P_{sat}$ or $-P_{sat}$ state. This effect has been related to reduction in the polarization switching due to the specific resistivity (Ω-cm) of the material and is similar to the previously discussed space charge driven theory of aging [Ref. 21: p. 1241]. As resistivity increases, the migration of the space charge produced by impurities is suppressed. This can contribute to loss of data due to the switching polarization reduced read capabilities.

In summary, aging and fatigue are the primary problems to overcome for memory applications of ferroelectric devices. The inter-relationship between aging and fatigue prevents treating these as independent problems to be solved separately. There are also several independent mechanisms which contribute to changes in material properties. In addition, testing procedures have a significant impact on the results obtained. The complexity of the inter-relationships and lack of testing standards contribute to the lack of consistency in experimental results. This not only complicates the fabrication of ferroelectric memory devices but increases risk and cost of fabrication. The consumer industry will lack confidence in the quality and reliability of the product when there is no firm theoretical support for this technology.

4. Ferroelectric RAM Design

a. Generic Two-Transistor

This is a conservative memory design which utilizes two pass transistors to shield the ferroelectric capacitor from capacitive feed-through when the word line is taken high. See Figure 2.9. If the ferroelectric capacitor is resistant to disturbance problems, the transistor on the drive line can be eliminated. The bit, word and drive lines are held at ground to isolate the ferroelectric capacitor. The "write" operation is initiated by making the word line

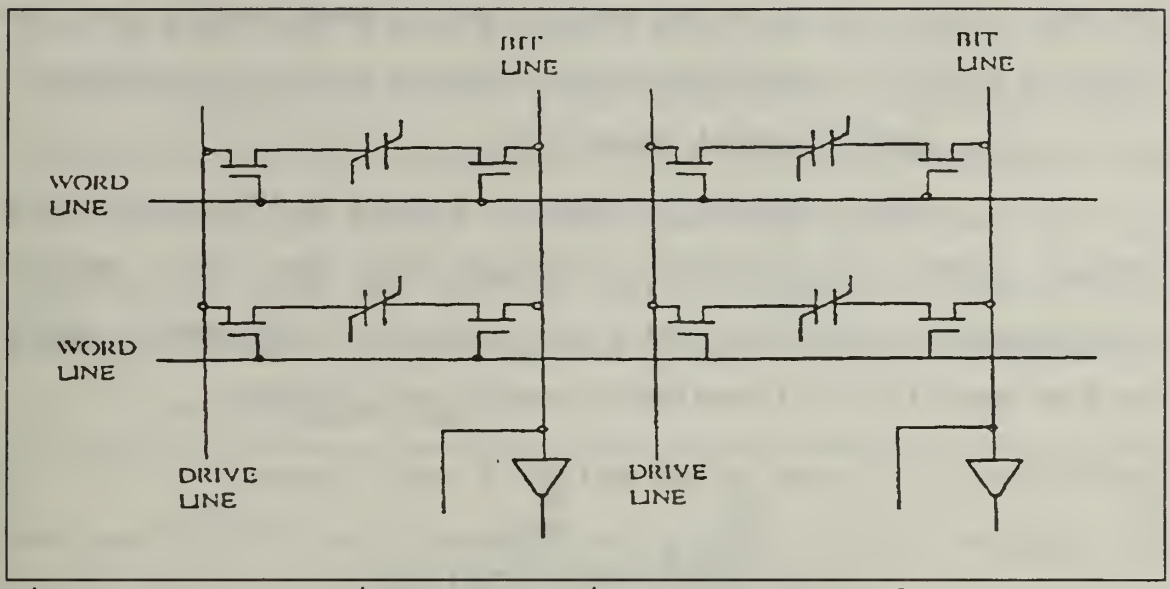


Figure 2.9: Generic Two-Transistor Memory cell [Ref. 4]

high, connecting the bit and drive lines to all the capacitors in that row. To write a "1", the bit line is made high, and to write a "0", the drive line is made high. To complete the "write", all lines made high are connected to ground. The "read" operation is initiated by making the word line high for the appropriate row. Then the drive line in the cell column is pulsed or made high for a short time. If a "0" is read, the polarity of the capacitor does not switch and the bit line will stay below an established voltage threshold. If however there was a "1" read, the switch in polarity causes the noninverting amplifier on the bit line to go high as the bit line voltage exceeds the threshold. The original "1" state is restored by output feed back to the bit line. The "read" operation is completed by returning all lines made high to

ground. Note that this DRO memory design must ensure that the restore cycle is completed before lockout occurs on powerdown.

b. Differential Read-Cell

This design, given in Figure 2.10, provides a larger signal differential through the use of a second ferroelectric capacitor and a bit line (BL) (complement) added to the generic two-transistor memory cell design.

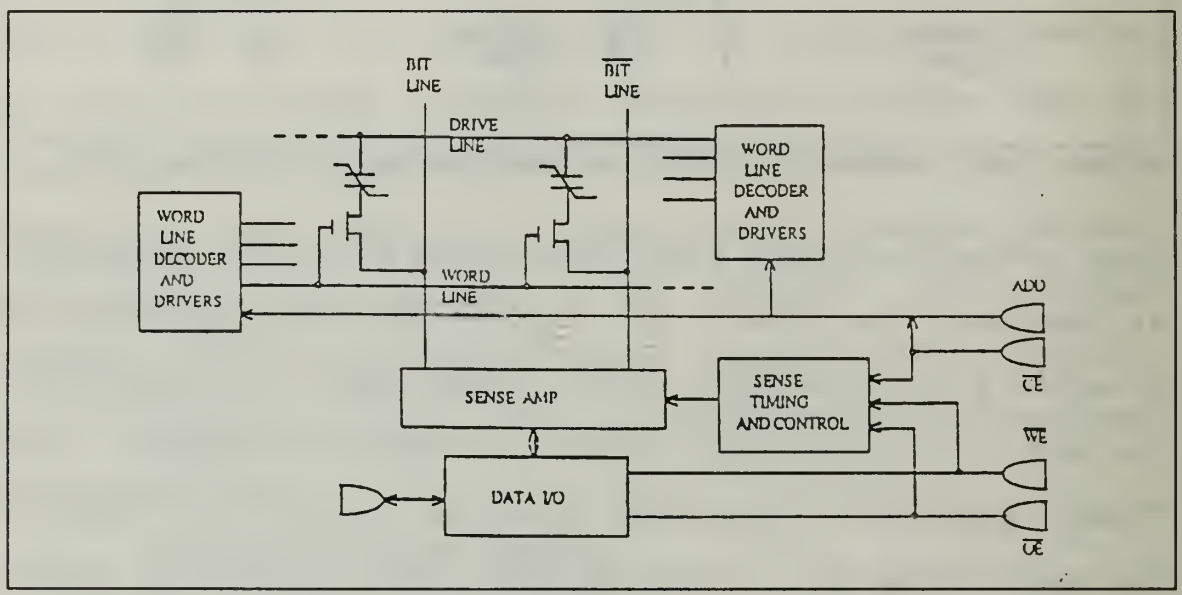


Figure 2.10: Differential Read Memory Cell [Ref. 4]

During a "write", the appropriate word line is made high and the sense amp is set to the desired state, driving the BL and BL complement to opposite voltages of ground and V_{drive}. The drive line is then made high to write a "0" to the capacitor at ground. When the drive line returns to ground, the second complementary capacitor is written with a "1". The state is that of the capacitor controlled by the BL. For the "read" operation, the sense amp is off, the word

line is made high for the appropriate row and the drive line is taken high. The paired capacitors are in opposite states therefore BL and BL (complement) have different voltages. The bit line with the higher voltage (switched capacitor) will go high as the sense amp turns on and the other bit line will be forced to ground, recreating the original write condition.

c. "Shadow" RAM

Ramtron has a design which uses a ferroelectric storage circuit as a "shadow" to a SRAM circuit through the use of control transistors. These transistors connect the ferroelectric capacitors to the SRAM cell and deselect the ferroelectric memory device to prevent data contamination when there is a power interrupt or power failure. When the control transistors are turned on, the ferroelectric capacitors are polarized to the appropriate state within approximately 20ns, well before the SRAM portion of the device loses its data due to power loss [Ref. 4]. When the control transistors are off, the device acts like a standard SRAM. After the data is stored in the ferroelectric array it can be recalled when power is restored or new data can be loaded into the SRAM cell while the old information is left in the ferroelectric array for later use. This design avoids the problem of fatigue since the ferroelectric capacitors are switched only when power is interrupted.

d. Ferroelectric Memory FET (FEMFET)

The ferroelectric memory field effect transistor (FEMFET) is a nonvolatile memory transistor whose threshold voltage is determined by the polarization of the ferroelectric comprising the gate dielectric [Ref. 19]. The ferroelectric material, sandwiched between two nonswitching dielectric layers, replaces the oxide layer and is used to regulate the conductivity of the semiconductor channel between the source and drain. The polarization state of the ferroelectric will change the electron population at the interface. For a p-type channel, a negative polarization will decrease the electron concentration and increase conduction while a positive polarization has the opposite effect, effectively turning off the FET. Since the polarization state is not altered to do a "read", the FEMFET is intrinsically a NDRO device which makes it much more preferable than traditional DRO devices. Additionally, only one FET is required per memory cell so there is potential for high density memory storage.

There are some design problems to overcome. It is difficult to fabricate the low resistance electrodes needed to get low voltage operation and it is difficult to deposit the ferroelectric film directly on silicon. Movement compensation charge throughout the ferroelectric film reduces the difference between the "1" and "0" voltages [Ref. 4].

e. *FRAM*

Ramtron has developed a viable proprietary ferroelectric compound, a complex thin film ceramic consisting primarily of Lead Zironate Titanate, which is compatible with standard semiconductor fabrication techniques. This thin film ceramic layer is integrated into an existing semiconductor process as shown in Figure 2.11.

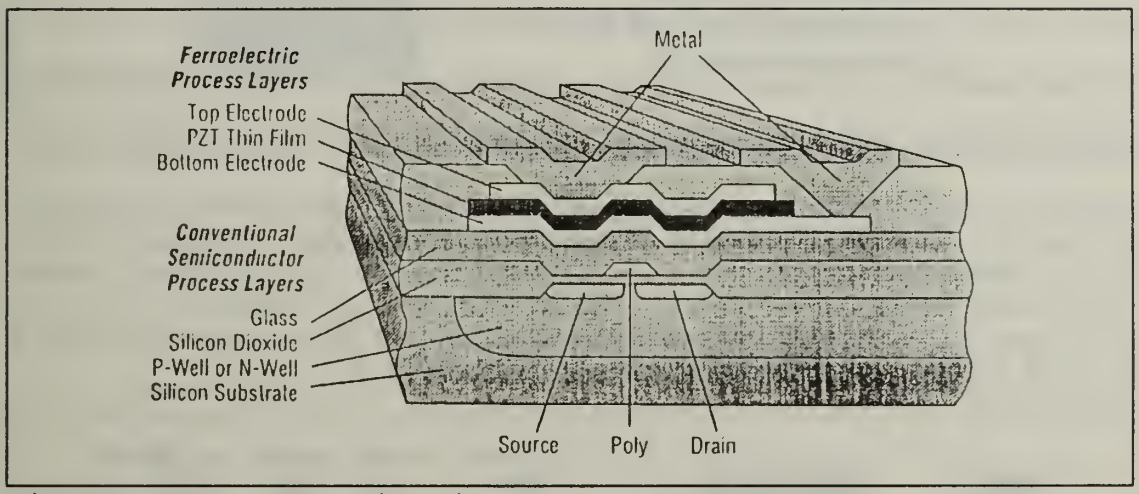


Figure 2.11: PZT thin film on CMOS [Ref. 10]

A ferroelectric RAM or FRAM memory is built by replacing the conventional capacitor in a standard DRAM circuit with a thin-film ferroelectric capacitor as shown in Figure 2.12. This creates for the first time a memory with the read/write performance and virtual unlimited endurance of the DRAM and the nonvolatility of magnetic storage. The FRAM memory has the potential to achieve the density and manufacturing economics of the DRAM.

Ramtron makes the FMx 1208, 1408, 1608 and 1808 integrated FRAM devices capable of 4,096-bit, 16,384-bit,

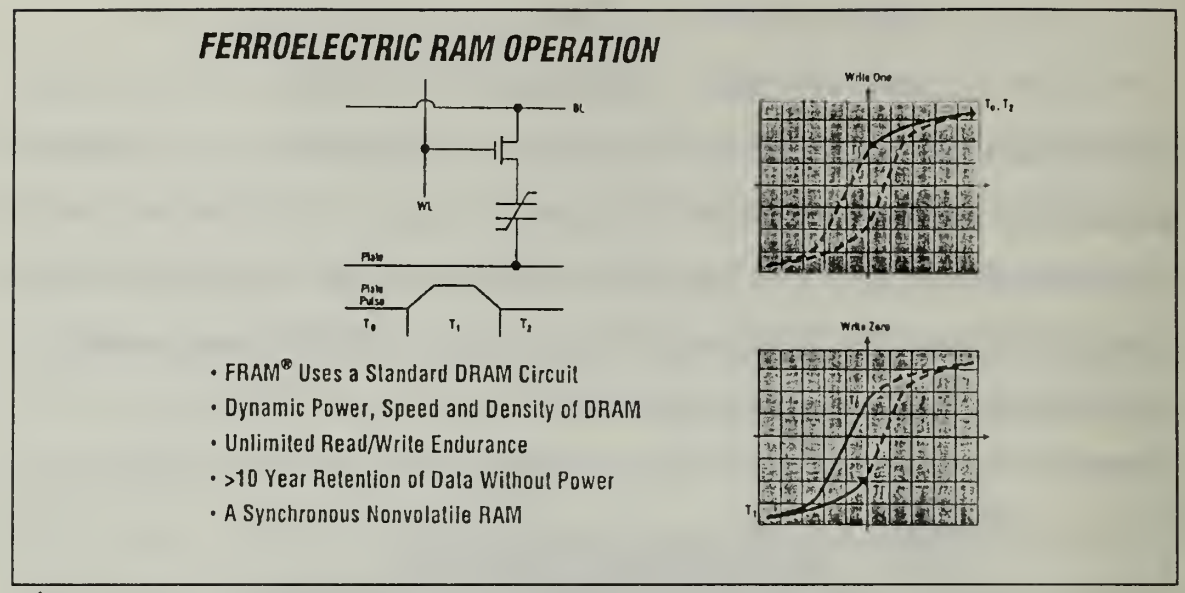


Figure 2.12: FRAM Cell [Ref. 10]

65,536-bit and 262,144-bit nonvolatile storage, respectively. A FMx 2008 capable of over 1 Mbit storage is currently on the drawing board as can be seen in Figure 2.13.

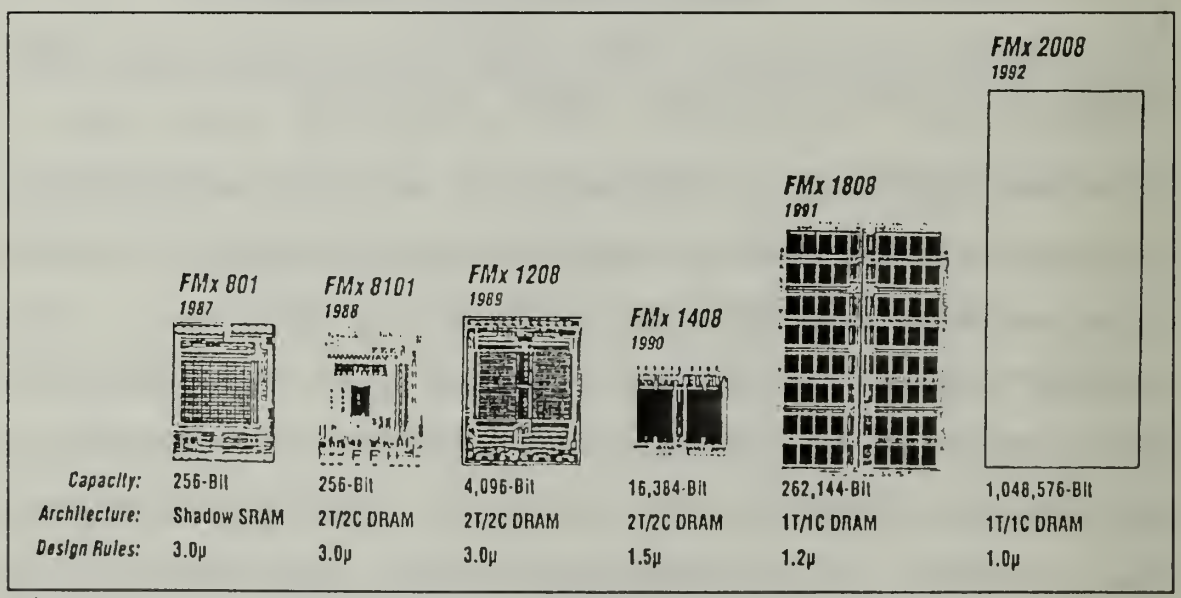


Figure 2.13: FRAM product evolution [Ref. 10]

FRAM is capable of two operating modes, dynamic and nonvolatile. The dynamic mode utilizes the high

dielectric constant of the ferroelectric cells to store data as an electrical charge. The data must be periodically refreshed, identically to conventional DRAMs, and read/write endurance is unlimited. In the nonvolatile mode, refresh operations to all addresses prior to a power loss cause the ferroelectric cells to spontaneously polarize, thereby retaining data indefinitely without power.

Ramtron believes, due to the small size, fast intrinsic switching speed, low energy requirements, nonvolatile mode of operation and the ability to obtain DRAM density with fewer manufacturing steps, FRAM is the "ideal" memory capable of consolidating all memory requirements into a single component as illustrated in Figures 2.14, and 2.15.

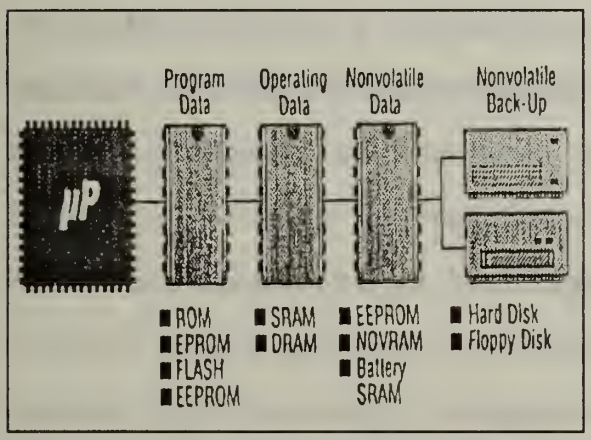


Figure 2.14: Many memories are needed to meet current system requirements [Ref. 10]

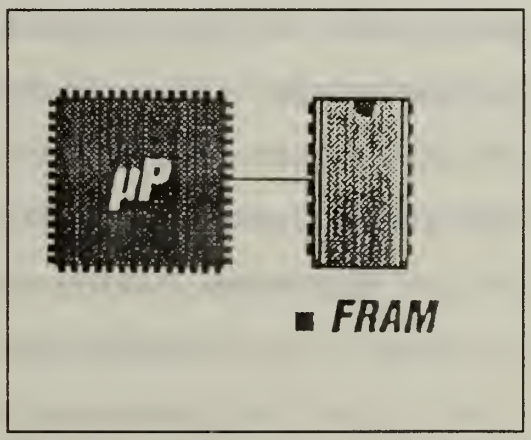


Figure 2.15: FRAM consolidates all memory requirements into a single component, providing an extremely simplified computer memory system architecture [Ref. 10]

f. One Transistor-One Capacitor

Seiko Epson and Ramtron are jointly developing a 256k-bit nonvolatile ferroelectric memory using a one transistor-one capacitor (1T/1C) memory cell approach. This technology uses 1.1μm CMOS technology with two levels of aluminum interconnect passivated with plasma silicon nitride. Integrated into the standard CMOS process modules are four additional mask steps which define the integrated ferroelectric capacitor storage element. The capacitor is 3.6μm^2 using PZT as a dielectric. The design allows the memory to operate as a conventional volatile DRAM using the linear charge of the ferroelectric capacitor or as a nonvolatile FRAM using the polarization charge. Typical properties of the capacitor include a permittivity of approximately 1100, polarization switching charge of 20$\mu C/cm^2$ at 5 V, a coercive voltage of less than 2 V and a leakage current of less than 100nA/cm^2 [Ref. 30].

g. Other Design Concepts and Applications

(1) Bipolar Memory

Raytheon is developing a ferroelectric memory based on bipolar rather than CMOS technology because of possible design and fabrication advantages. Bipolar devices are current driven rather than voltage driven so the switching current can be directly sensed without conversion to voltage. This may provide better detection threshold values, although

higher power will be required. Bipolar device can withstand higher temperature-procedures during fabrication, allowing optimization of ferroelectric properties. Also, bipolar circuitry is less sensitive to total dose ionizing radiation [Ref. 4].

(2) Analog Memory

Somewhat similar in design to bipolar memory, analog memory relies on the ability to control the degree of switched charge in ferroelectrics. By applying a pulse of insufficient amplitude (i.e. an electric field E which is less than E_c) and/or duration to a ferroelectric device, it can be partially switched. A smaller hysteresis loop can be observed with the shape and stability dependent on the material characteristics and the frequency and magnitude of the applied field. Consequently, an analog memory device which would be suitable for use in IC neural networks and other applications requiring storage of analog values may be fabricated. The measurement of analog switching is difficult but a custom voltage pulse generator capable of generating the requisite waveforms with sufficient drive and speed has been built [Ref. 20]. A possible application is a neural network synapse incorporating a metal-ferroelectric-metal capacitor circuit. The switching behavior could also be exploited for an NDRO design, using circuit voltage levels such that the remanent polarization is moved to a smaller level, but not switched,

for the read operation. The normal process could then be used to restore the memory capacitor to its original remanent polarization state [Ref. 4].

(3) Latch

Krysalis, now absorbed by National Semiconductor, developed a nonvolatile octal D-type flip-flop with nonvolatile recall of stored data after power off. It functions as a standard 8-bit latch with the added feature of nonvolatile data storage on each positive clock transition. This provides automatic data protection in case of power loss. The device is being evaluated for applications such as automobile odometers, access counters, and flight time recorders [Ref. 4].

(4) Optical Read

Changing the electrical polarization of ferroelectric materials will also change some of their optical properties, including changing the birefringence (double refraction), refractive index and the transparency of the material [Ref. 4, Ref. 27]. For memory applications, data storage is done by setting the desired polarization state with an applied electric field and optical data recovery. The simplest form of optical memory is an electrically controlled light valve. Recalling how a cubic unit cell is stretched along the vertical axis and shrunk along the two other vertical axes by an electric polarizing field, an optical

polarizer can be aligned at the input of one horizontal axis to allow light to propagate through. The polarization of the vertical axis only is reversed by the application of an electric field. An analyzer at the output of the electrical dipole polarization state of the sample can be determined by the magnitude of transmitted light [Ref. 4]. This electrical "write" and optical "read" offers NDRO qualities to such a device.

One could take this technology even further to design components for optoelectronic computing systems. Example of optoelectronic components include smart spatial light modulators and holographic storage modules. The University of California, San Diego is currently attempting to construct a 4096 parallel processor [Ref. 27]. This parallel processor consists of 4096x4096 free-space cross connects using the photo refractive properties of ferroelectric materials. To operate the processor, smart spacial light modulators capable of greater than 10:1 interconnect ratios, 5% modulation depth and 10 MHz switching speeds are being designed.

(5) Pressure/Velocity Sensors

The University of Minnesota has developed several design and process considerations for producing piezoelectric pressure microsensors using existing sol-gel derived ferroelectric thin films [Ref. 28]. Piezoelectric

charge detection using ferroelectric thin film-based sensors is a viable scheme for sensing pressure variations in the acoustic range (100-20,000 Hz). They are produced by dielectric stacking deformable membranes above the surface of a silicon substrate, onto which an active sensing ferroelectric film element is deposited and patterned. The dielectric stack is spaced off from the substrate surface, allowing it to respond readily to mechanical stresses. The selection of electrodes and insulating materials can affect the pressure sensitivity. Piezoelectric pressure sensors have already demonstrated the ability to detect pressure variations alternating with frequencies in the acoustic range (100-20,000 Hz). This type of pressure sensor has the great advantage of directly converting acoustic energy into electrical energy. No external power is consumed by the sensor. The power needed for operation is solely that consumed by the amplifier circuit and can be minimized using CMOS design.

Researchers at the University of Colorado have discovered an unusual form of optical bistability in hot-pressed ceramic PMN ($PbMgO_3NbO_6TiO_1O_3$) in which the thermal focussing of laser light at very low power densities (< 1 kW/cm^2) oscillates between two metastable states [Ref. 29]. At low laser powers the phenomenon is highly aperiodic but extremely reproducible. The oscillation events occur at times t_N empirically given by the equation $t_N=A[Jules]/(P-P_N)$, where

the threshold power P_N for the N^{th} switching event is found to be $N \cdot P_o$, where P_o= 45 mW (i.e. 3.6 W/cm^2 power density). At higher laser power the switching events become periodic. One of the two metastable light patterns is doughnut shaped and the other resembles a Bessel function, with a large intensity in the center. By setting a Si-diode detector in the center of the pattern, the oscillation can be monitored. The frequency of the oscillation events is strongly dependent upon convection from the sides of the PMN thermal lens. Therefore the device acts like an optical sensor that is extremely sensitive to pressure and flow rate of the surrounding atmosphere. Pressure changes of 10^{-2} Torr and flow rate changes of 0.1 ft^3/hr (0.3 m^3/sec) in air have been measured with such a device.

(6) Ferroelectric LCD

Ferroelectric Liquid Crystal Displays (FLCDs) are already entering the market [Ref. 26]. *Canon* is the first to commercialize this technology and will use monochrome FLCDs in some of its own products this spring. There are plans to make available this fall a 15 inch (1280-by-1024 pixel) color monitor for desk top computers. In the future, FLCDs will be used for portable computers and thin HDTVs.

The FLCD's mechanism is essentially the same as that of conventional LCDs. In conjunction with polarizers that orient light in certain planes, liquid-crystal molecules

are aligned to either block light or let it pass. Alignment of the liquid crystal is controlled by passing an electric charge through them. Conventional LCD technology requires a continuous current to maintain the crystals open. Since FLCDs are bistable, they require only a single brief charge to align the crystals in the open or closed position. FLCDs also have high resolution and faster response time than conventional LCDs. The size of the FLCD panel doesn't affect the resolution unlike conventional LCDs and switching times are twice as fast (50-100ns). The only two weak points with FLCDs are the power consumption and shock resistance, but Canon is working on this.

(7) Thermal Imaging Arrays

Conventional arrays of photon detectors need high speed mechanical scanners and a significant amount of cooling, resulting in an expensive and complex system. A non-scanned, two dimensional array of pyroelectric detectors provide reasonable performance with simple, uncooled operation [Ref. 31]. The result is a light-weight and cost effective thermal imaging system. A temperature resolution of 0.25°K (F1 optics, 300°K scene, 8-14 μm wavelength) has already been observed in a 100x100 detector array. The detector is a $1cm^2$ pyroelectric chip, divided into a 100x100 array of individual elements. Each element of the array corresponds to a fixed solid angle, collecting power according to the scene

temperature and emissivity. By periodically interrupting the radiation with a mechanical chopper, the detector element temperature can be modulated. The detector material is pyroelectric, so it produces a voltage signal proportional to this temperature modulation, providing the data required to generate an image of the scene. A thermal imaging system is simple to fabricate with high yield and is simple to operate, as may be required for a short range hand held camera.

(8) Piezodevices

Piezoelectric materials have a wide variety of applications. One of the most mature is the commercial production acoustic transducers ranging from low frequency Naval hydrophones to high frequency medical ultrasonic imaging transducers [Ref. 32]. Since useful piezoelectric materials are insulators, their electrical impedance is due to primarily their capacitance. In most acoustic applications, the piezoelectrics are used in the form of large thin plates, so the device capacitance, C, is just the effective dielectric constant, ϵ, of the material times the plate's area, A, divided by its thickness, d (see equation 3 where $\epsilon=\kappa\cdot\epsilon_o$). The dielectric constant is the material property of interest; all other parameters are determined by device design. The acoustic impedance is the sound wave analogue to the index of refraction for light waves. It should be closely matched to

the medium into which it is projecting, or from which it is receiving, sound waves (i.e. water or human tissue).

An innovative new technology applicable to micro-electronic circuits is a piezoelectric, battery driven, IC controlled, mW ultrasonic Kumada motor [Ref. 33]. Different from conventional electromagnetic motors, ultrasonic motors can operate at less than 0.1 Watt of power. Ordinary magnetic motors have a disadvantage in that the power and size reduction causes high speed rotation but with too small a torque. The Kumada motor is based on a stator consisting of a piezoelectric revolving resonator. Its center of mass rotates around the geometric center drawing a circle with a few μm in radius, at a very high speed of about 1 million rpm. The big advantage of this motor is its direct drive; the moving part of the system is the rotor itself.

An interesting development involving ceramic actuators is in the application of shape memory effect [Ref. 35]. The shape memory effect phenomenon involves the phase transition between ferroelectric and antiferroelectric states in ceramics of Lead Zirconate, modified with Titanium (Ti) and Tin (Sn), abbreviated as PNZST. The phase transition from antiferroelectric to ferroelectric states produces a strain, which increases abruptly by increasing the applied electric field. The strain decreases and returns to the initial state with a decreasing field in certain PNZST. When the Ti and Sn concentration ratios are properly set, the field induced

strain will not diminish despite the decreasing electric field. This is the shape memory effect and a slightly reverse bias field is needed for recovering the strain. By controlling the shape memory of PNZST, new devices such as latching-relays or mechanical clampers can be fabricated [Ref. 36]. In comparison with the conventional piezoelectric actuators, the newly developed ceramic has advantages such as three times larger strains and energy saving drive by a pulse electric field.

5. Memory Applications

a. Conventional Memory Disadvantages

There are several systems requiring nonvolatile memory and as these systems become more complex, the demand for reprogrammable nonvolatile memory increases. The complexity and cost in making conventional nonvolatile memory reprogrammable also increases, so the potential for using ferroelectric memory as a replacement will increase as well. As previously noted, FRAM can be used to replace all RAM and EEPROM devices. Several of the ferroelectric memory designs already mentioned have been compatible with existing EEPROM pin-outs, allowing simple replacement and integration with existing circuit designs.

Conventional nonvolatile memories have disadvantages that can be overcome by switching to ferroelectric memory [Ref. 4]. ROM and PROM have excellent

endurance but are not designed to be easily reprogrammed. Magnetic core memory offers radiation tolerance but is slow, bulky and power hungry. Magnetic bubble memory is an improvement but still requires more space and power than current semiconductor memory. EPROM can be erased and reprogrammed but requires a great deal of time and inconvenience to physically place it under a UV light. EEPROM can be electrically reprogrammed in place but it is limited to 10^5 rewrites and still requires too much time. SRAM is fast but requires a battery back-up and because it uses six transistors, storage densities are low.

b. Applications for Ferroelectric Memory

Commercial applications for ferroelectric memory devices are as numerous as there are innovative scientists and engineers. The technology is currently being used in video games, toll-booth car tags and credit cards that automatically keep track of your account. It could easily be used for printers, I/O configured memory and in compact cellular phones. Ferroelectric memory can be used to fabricate neural nets for neurocomputing and analog computers can be simplified with the aid of ferroelectric memory. Embedded controllers for any system or plant that requires constant and accurate changes to programming would benefit from ferroelectric memory. Ferroelectric memory chips could be used for electronic picture storage and notebook PC solid state disks.

Computer system memory architectures could be greatly simplified. Eventually, higher densities will make digital voice recording and on-line databases possible from a single memory chip.

The military applications are almost endless. Navigation and targeting information could be stored onboard the weapon such as cruise missiles, smart mines and torpedoes. For aircraft, airborne mission data storage, weapon system loadout information, electronic warfare suite setup parameters, maintenance records of inflight aircraft system parameters, remote-site inventory data collection and storage for supply records, weapons guidance and search parameter tailoring and recording of built in test (BIT) system results could be maintained to aid in shorter development times and more rigorous operational test and evaluation. Ferroelectric memories can be used for aircraft encrypted communication system and field radio encryption devices, providing both nonvolatility and extended endurance for frequent changes to key lists. Magnetic core memory, due to its rad-hard qualities, is still being used by the Space Shuttle, F-16, B-2 and EA-6B. By using ferroelectric memory, you can save considerable space, weight and power [Ref. 4].

c. High Radiation / Space Environment

Due to its inherent radiation tolerance, ferroelectric memory is ideally suited for use in satellite

memory design. The space environment where some satellites are positioned contain radiation belts, which consist of trapped electrons and ionized particles. The solar wind also generates charged particles that can damage electronic systems on board a spacecraft. Shielding sensitive electronic components from this radiation can add costly weight to the design. Therefore, components with inherent radiation hardness are used to the fullest extent possible. Ferroelectric memories could provide a semiconductor replacement for spaceborne tape recorders and should prove useful for long duration space missions where reprogrammable nonvolatile memory can allow adjustments to the mission profile.

In summary, ferroelectric materials used for memory applications must have several characteristics to be successful. They must maintain adequate remanent polarization, high switching speed, acceptable rates of fatigue and aging, CMOS-compatible coercive field, sufficient operating temperature range and compatibility with standard semiconductor IC fabrication methods. These criteria have narrowed the current list of materials to Barium Titanate ($BaTiO_3$), Lead Germanate ($Pb_5Ge_3O_{11}$), Barium Manganese Fluoride ($BaMgF_4$), Lithium Niobate ($LiNbO_3$) and the current favorite, PZT. If ferroelectric memory can become competitive with DRAM on a cost and density basis, the benefits of speed and

nonvolatility will be exploited to simplify computer system memory architectures.

A recent material showing excellent promise for DRAM capacitor application is $(Ba_{1-x}Sr_x)TiO_3$ [Ref. 14]. Most important, this material can be prepared in thin film form of stoichiometric composition with excellent reproduction capability using simple single target sputtering deposition techniques. This is in contrast with PZT where the lead content is difficult to control and therefore Sol-Gel or other sophisticated methods such as multi-target sputtering must be used to overcome this difficulty.

Recent claims have been made of a newly developed fatigue-free ferroelectric capacitor, including zinc doped PZT [Ref. 15, Ref. 16]. The change in properties for the fatigue-free capacitors were examined over a wide range of switching cycles (10 to 10^{11}) while keeping a well saturated hysteresis. There are still several materials left to evaluate and one may yet be discovered with significantly better properties. The potential is certainly there for ferroelectric memories to successively displace other memory technologies and become competitive with DRAMs as device densities increase beyond the point where DRAMs are scalable. However, before ferroelectric memories can seriously compete with existing technologies, startup manufacturers must resist the pressure to produce immediate results and make premature product announcements.

Although such optimism of being first has its rewards in an exciting and rapidly growing market, this can sometimes lead to skepticism and hesitation for potential users to take advantage of this technology.

III TESTING FERROELECTRIC CAPACITORS

There are currently numerous companies and joint industry-government-university research groups throughout the world actively involved in the testing of thin film ferroelectric ceramic technology for nonvolatile integrated circuit memory application. This is due primarily to the dramatic technical advancements in the ability to produce thin film perovskite ceramic ferroelectrics by using conventional integrated circuit fabrication techniques such as ion sputtering, liquid spinning, furnace and rapid thermal annealing, photolithography, wet etching and plasma etching, sol-gel chemistry and eximer laser ablation. Also of great interest is the fact that these materials are structurally similar to the recently discovered high temperature superconducting perovskite ceramics and that the phenomena of superconductivity and ferroelectricity in these materials may be related.

The primary focus in testing these new materials are a complete understanding of their properties such as stress, interfacial reactions, adhesion, electrical hysteresis properties, breakdown voltage, fatigue, reliability and the ability to generate computer simulation models for circuit simulation and memory design. Measurements that are

considered particularly important for analysis are curie temperature, frequency dependence on spontaneous polarization, saturation, maximum and remnant polarization, coercive field and relative dielectric constant. Also important is leakage current (an increase in leakage current can be mistaken for an increase in polarization), dielectric breakdown and time dependent dielectric breakdown, aging, fatiguing and retention (see Chapter II-B, Ferroelectrics Background). There are several testing systems and methods possible to make these types of measurements. Unfortunately, not all of them give consistent results.

A. MANUAL TESTING

1. High Frequency Fatigue Test

National Semiconductor employs a pulse generator connected to a PC to fatigue individual capacitors at 1MHz and automatically measure the polarization [Ref. 37]. The simplicity in design and flexibility in selecting cycling frequencies makes it appealing for fatigue testing. To test fatigue in a substantially shorter amount of time, National Semiconductor has also developed an in-house cycler capable of cycling ferroelectric capacitors at 6MHz [Ref. 37, Ref. 45]. Since large sense capacitors are used to avoid noise (caused by parasitics associated with the wiring) and get clean measures of remanent polarization, high speed cycling requires high current drive capabilities of pulse generators due to the

large capacitive loads. National's in-house cycler was specifically designed to drive multiple ferroelectric capacitors at 6MHz-25Ω and they have already measured fatigue characteristics beyond 10^{13} cycles on 100x100 and 20x20μm^2 capacitors. National has future plans for a 8MHz tester that can deliver 1 Amp of current [Ref. 45].

Arizona State University, funded by the Defense Advance Research Project Agency (DARPA) has developed a mercury wetted relay pulse generator [Ref. 41]. Test pulse characteristics (i.e. rise time and current drive) from commercial pulse generators depend on the size of the ferroelectric capacitor being measured. This limits the ability to compare various size samples. The mercury wetted relay pulse generator can deliver high current of 1 Amp at amplitudes of ±50 volts, with short pulse rise and fall times of 1ns to a 50Ω resistor. Most significant is that the output of this generator is independent of the sample being probed. An added advantage is the reduced signal reflection allowing for improved high speed switching measurements.

2. Virtual Ground Mode

McDonnel-Douglas Electronic Systems Company is one among many that now use a different testing method which doesn't involve the traditional Sawyer-Tower configuration [Ref. 38]. Due to its simplicity and low cost, the Sawyer-Tower circuit has been a common method for characterizing

ferroelectric devices. However it is susceptible to significant errors from parasitic elements usually associated with the sense capacitor hook-up, and it is limited by the accuracy to which the sense capacitor value is known. Consequently it may be difficult to calibrate and to compare results from different test set ups. A simple virtual ground circuit can be seen in Figure 3.1 [Ref. 39: p. 5-2]. The virtual ground mode measures the charge stored in the ferroelectric sample by integrating the current required to maintain one terminal of the sample at zero volts, hence the term "virtual" ground. By eliminating the external sense capacitor, this circuit drastically reduces the effects of parasitic elements. The precision capacitor used as the feedback element in the current integrator is now a key element in obtaining high accuracy with this technique. Using a train of positive-positive-negative-negative pulses as the driving voltage, then integrating the switched and non-switched pulses and finding the measured difference yields the switched charge (see equation (7)). For endurance tests, McDonnel-Douglas measures the switched charge in decade steps of accumulated switching cycles. The retention of the switched charge at each break point is measured by varying the interval between the write and read pulses. True measurements are the storage of data in the memory as a function of cycles and retention time. This measurement is made for both "1" and "0" storage at each location with truth table readout. Using

the virtual ground mode allows device characterization with improved accuracy and allows results obtained from different test set ups to be compared with confidence.

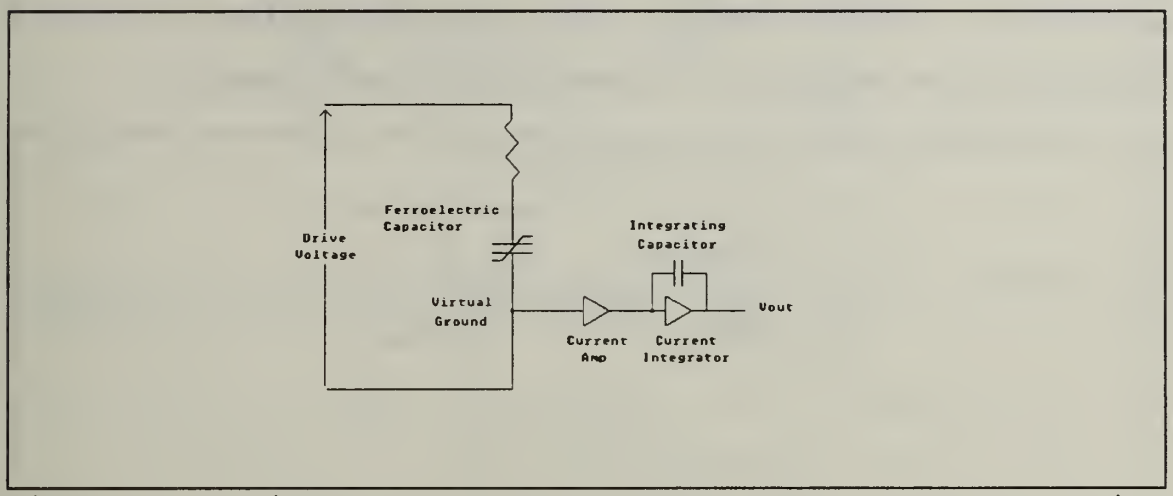


Figure 3.1: Virtual Ground Test Method [Ref. 39: p. 5-4, Fig. 5-3.

3. High Precision Test Systems

Although polarization cannot be measured directly, the Sawyer-Tower circuit is useful for identifying trends, since the constant measurement error will not obscure a loss of polarization due to fatigue or ageing. When exact measurement of polarization is required, there are other circuits available for more precise measurements.

a. Compensation Circuit

A compensation circuit involves using a standard Sawyer-Tower circuit with another redundant Sawyer-Tower circuit arranged in bridge fashion as shown in Figure 3.2 [Ref. 37: p.222, Fig. 2]. The redundant Sawyer-Tower circuit

has an adjustable capacitor and adjustable resistor to allow conductance of the ferroelectric capacitor to be subtracted from the overall measurement by use of a differential amplifier. Unfortunately, this circuit requires time and patience to be manually adjusted for proper operation.

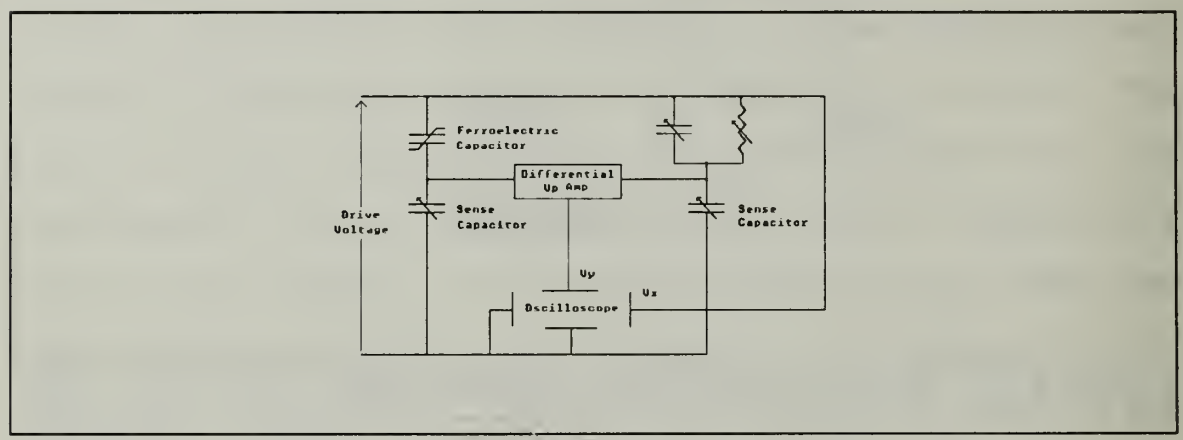


Figure 3.2: Compensation Circuit [Ref. 37]

b. Modified Virtual Ground Circuit

The modified virtual ground circuit shown in Figure 3.3 includes the compensation circuit mentioned previously and also employs the virtual ground of an operational amplifier to eliminate measurement distortion caused by conduction in the sense capacitor [Ref. 37: p.223, Fig. 3]. The current amplifier and integrator stages of the virtual ground circuit is designed to minimize gain and offset errors. They can also be calibrated in order to standardize measurements and can be recalibrated as needed to compensate for drift or changes in the test set up.

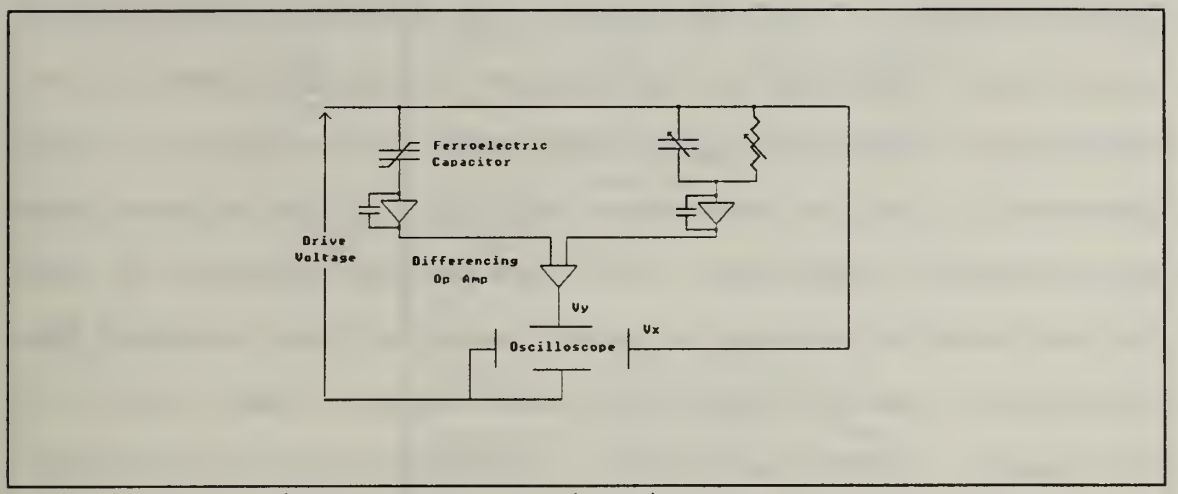


Figure 3.3: Virtual Ground Circuit [Ref. 37]

B. AUTOMATED TESTING

1. Stress Measurement System (SMS)

a. Original SMS

The Stress Measurement System (SMS) was designed and built in 1989 by Gordon Force of Force Technologies, San Jose, under contract from Krysalis Corporation [Ref. 9, Ref. 37, Ref. 40]. It is the result from a joint project of Krysalis and the Ferroelectric Group of National Semiconductor Corporation to develop thin film ferroelectric products. The system delivered by Force Technology consisted of eight nearly identical test boards, each suitable for placement in a 16MHz 80286 IBM PC host computer. It also included four extension boards with remote jigs for use in a test oven rated to 125°C [Ref. 40]. The purpose of the SMS tester was to do automated

stress testing (cycling tests) of on-chip ferroelectric capacitors. The SMS was then tailored for the ferroelectric capacitors fabricated by National Semiconductor, which consisted of two Devices Under Test (D), each D holding seven ferroelectric capacitors. The SMS was not designed to test devices such as latches or actual memories that included CMOS circuitry. The SMS incorporates the Sawyer-Tower circuit in its design (see Figure 2.5). It cycles the ferroelectric capacitors, writes voltages to them and reads the capacitor at specific times at specific voltages to measure digitally the switched charge (see Chapter II-B-2-c&d). The SMS can also send 180kHz bipolar square pulses for fatigue testing. Software for the SMS was written in "C" by Force Technology but was subsequently modified by engineers at National Semiconductor. The original program was 15 pages in length and required the test operator to enter a "main()" function and write a test program using four other primary functions. The microcontroller of the host PC is used for the 1μs resolution timing pulses required on the circuit board, so a major limitation of the SMS is its requirement to use only a 16MHz 80286 dedicated PC.

The board itself is 7"x11"x1¼, and requires an external power source that can deliver +15 to -15 volts. The block diagram of the system appears in Figure 3.4. The original system was comprised of 12 functional elements or blocks. Block 1 is the host PC (IBM or compatible with a hard

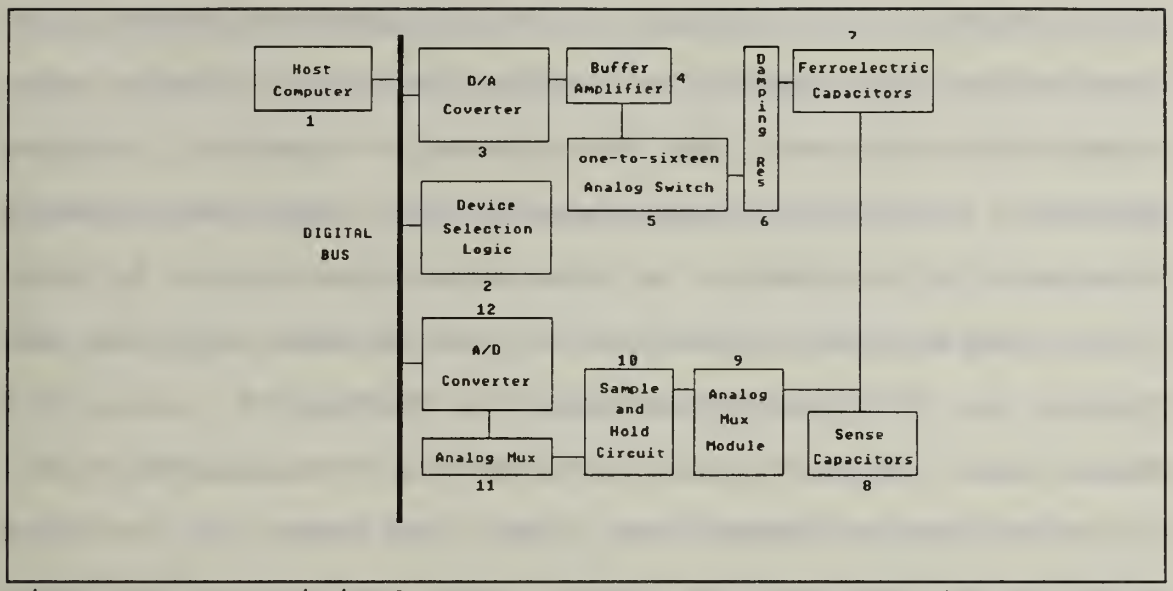


Figure 3.4: Original Stress Measurement System (SMS), Force Technology Corp. [Ref. 40]

disk drive). The printed circuit board for the SMS system consists of blocks 2 through 12.

Write pulses are applied when the ferroelectric capacitor is electrically isolated from its sense capacitor. This is necessary to insure that the voltage applied to the ferroelectric capacitor is not shared in a voltage divider circuit with the sense capacitor. The correct technique for isolating a ferroelectric capacitor is to provide a direct path to analog ground from the sense node of each ferroelectric-sense capacitor junction. This path to ground shunts the sense capacitor out of the active circuit (see "Improved" SMS). Read pulses are used to test the magnitude and polarization state of the ferroelectric capacitor. Before sending a read pulse, the ferroelectric capacitor and the sense capacitor are placed in series by opening the sense node

or junction to analog ground. A read pulse is sent and about 20μseconds is allowed to elapse to fully charge both capacitors, whether the ferroelectric capacitor changes polarity within that 20μseconds or not. The total charge created will accumulate at the sense node shared by both capacitors and while the read voltage is still applied, the sample and hold device measures the voltage V_o across the sense node. Another 20μseconds later the sense capacitor will fully discharge through the sample and hold and the read voltage is returned to zero. The sense node is then disconnected from sample and hold and reconnected to the analog ground to isolate the ferroelectric capacitor during cycling [Ref. 40].

b. "Improved" SMS

After Krysalis Corporation was bought out by National Semiconductor Corporation in 1989, William R. Hestir, a thesis student from the Naval Postgraduate School, began an experience tour with the engineers at National's Ferroelectric Process Group. He was assigned the project of discovering why the SMS tester produced verifiable results when measuring a single D, but produced highly variable data when more than one D was measured. When multiple D tests were conducted, there was an apparent polarization loss seen in all but one of the DUTs measured [Ref. 40]. It was discovered that the SMS was only capable of grounding one D at a time. The DUTs that were

not grounded were still attached to their sense nodes, which were a source of unwanted floating voltage from the external circuit. Since the charge at the sense node was being altered, subsequent measurements appeared to show an ageing loss in the ferroelectric material. This ageing loss could not be duplicated when the D was tested individually.

To provide a proper route to ground for each of the 16 DUTs the SMS tester was redesigned to hold, 32 analog switches to ground and their associated control logic was inserted between the device selection logic and the capacitor sense node as seen in Figure 3.5.

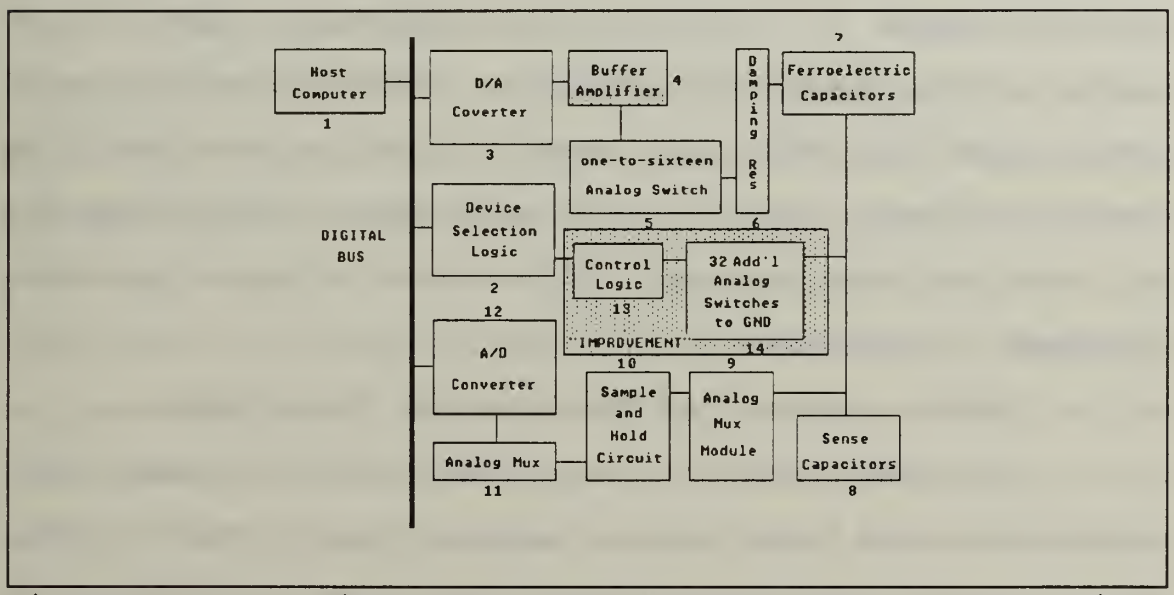


Figure 3.5: The improved Stress Measurement System consists of an additional board holding analog switches for the ferroelectric and sense capacitor junction.

The "improvement" was simply a connecting jig and a separate board that linked each sense node (112) on the original board to ground via an LF201 "normally-closed" analog switch.

Normally-closed implies that the ferroelectric capacitor should always be grounded unless it is in series with the sense capacitor for a read.

Limitations for the SMS and subsequent modifications are due to the limited scope of testing that the SMS was designed for. To test fatigue in a reasonable amount of time, greater cycling speeds than the 180kHz used by the SMS must be used. To reach 10^{13} cycles for example it would take 643 days at 180kHz where it would take only 29 days at say 4MHz. Current SMS design also requires 112 large sense capacitors to take up valuable real estate on the printed circuit board. To test for radiation hardness of ferroelectric capacitors, CMOS test control circuitry must remain off the test chip where it can be shielded from radiation damage. This could involve using a connecting jig or using radiation hardened components to minimize shielding thickness required.

2. RT66A Standardized Ferroelectric Test System

Raytheon Equipment Development Division, among other laboratories and universities, use an extremely user friendly RT66A Standardized Ferroelectric Test System developed by Radiant Technologies Inc. [Ref. 39]. The RT66A was specifically designed to perform the tests required for characterizing non-linear ferroelectric thin films of specific bulk ceramic devices. It combines the features of a function

generator, an electrometer, and a digital oscilloscope in a single package. The tester is controlled by an IBM PC or compatible and the user specifies the operations which the tester is to perform from a menu driven interface. The RT66A software then executes the appropriate hardware commands, collects and processes the data, and then displays the results on the user's screen.

The standard software programs allow the user to perform hysteresis, pulse response and bipolar resistivity measurements. It allows the user to define the drive profile used in the tests, measure changes in resistivity due to long term DC bias and measure the effects of fatigue on the ferroelectric capacitor. After each fatigue period a pulse polarization measurement is performed on the test sample. The fatigue pulses may be either internally generated or provided externally by the user. Additional software allows for measurement of ageing, retention loss and stress. Hardware accessories include a High Voltage Interface (HVI) which allows the user to test any capacitive sample up to 4000 volts without fear of test equipment damage, and a 24:1 Multiplexer (Mux) which expands the number of controllable outputs for the RT66A, allowing the user to connect up to 24 samples simultaneously to the tester.

The RT66A was designed to be a "flexible" test system. The flexibility refers to the ability to place most test unit functions under software control. This allows test unit

operations to be user driven and therefore easily modified by the user to accommodate standardized tests as they are developed and defined. A block diagram of the RT66A test unit is shown in Figure 3.6.

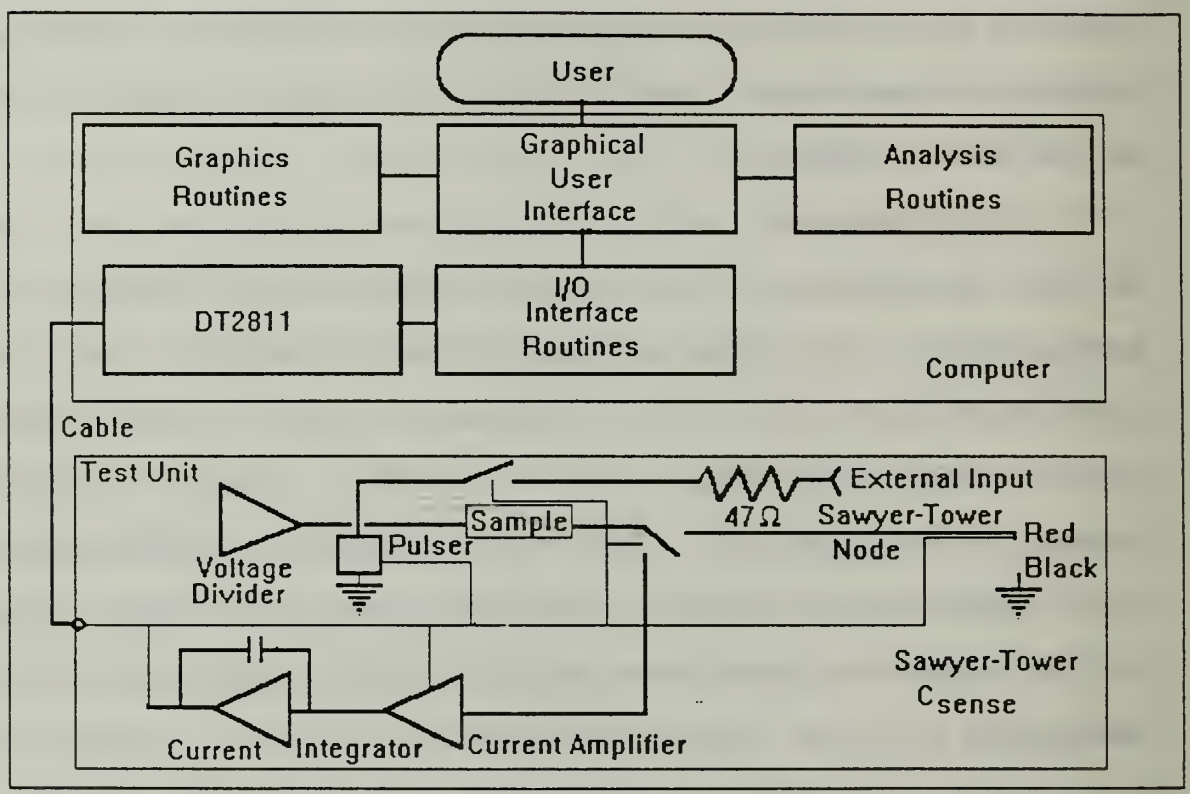


Figure 3.6: RT66A Test Unit Block Diagram [Ref. 39: p. 5-3, Fig. 5-1]

The host computer runs the graphical user interface, sends commands to the test unit, processes the measured data and displays the results on the computer screen. The host computer communicates with the test unit through the Data Translation (DT2811) interface board. The DT2811 has digital input/output (I/O) lines and both analog-to-digital (A/D) and digital-to-analog (D/A) converters built in. The digital I/O lines allow the host computer to perform as the test unit's

controller by setting and sensing hardware states and triggering hardware driven events. The D/A outputs are buffered and amplified by the test unit to drive the sample. The A/D channels are used to measure values at the voltage driver, Sawyer-Tower node and the current integrator. The two available testing modes, Virtual Ground and Sawyer-Tower, provide two standard means of testing ferroelectric materials [Ref. 39: p. 5-1].

3. Space Application Testing

Ferroelectric thin film capacitor devices irradiated using x-ray and Co-60 sources to dose levels in excess of 10 Mrad(Si) have shown good radiation resistance, but not much is known of the effects of high energy charged particles such as energetic electron or proton bombardment that are of particular importance to space missions [Ref. 49]

a. Ferroelectronics (FERRO) Experiment

The Advanced Photovoltaic Electronics eXperiment (APEX), developed by Orbital Sciences Corporation (OSC), is scheduled for launch on a Pegasus launch vehicle in December, 1992 [Ref. 43]. The APEX orbit (70° inclination, elliptical) will provide access to high doses of ionizing radiation in the lower Van Allen belt, primarily in the form of trapped solar wind protons of energies less than 10MeV. The APEX mission consists of three independent experiments. The primary one is the Photovoltaic Array Space Power plus Diagnostics (PASP-

PLUS), developed by NASA/Goddard Space Flight Center. A second experiment is the Cosmic Ray Upset Experiment (CRUX), developed by the Air Force Geophysics Laboratory. The third and smallest experiment is FERRO. The objective of the FERRO experiment is to autonomously measure the cycling fatigue and aging response of integrated ferroelectric capacitor devices in the space environment. Four ferroelectric capacitor ICs are integrated into the experiment module and each will be tested under the control of the system software.

The FERRO experiment consists of four major subsystems; the Device Under Test (D) board, the microprocessor based controller board, the experiment housing and the system software. The D boards carry four ferroelectric capacitor ICs (Ramtron's KFATQ3 devices) and associated support electronics. The D board design is modeled after the SMS board mentioned previously. The microprocessor based subsystem is composed of a fully configured M80C196KB microcontroller (military version of MCS-96) and associated peripherals. All system control and logic functions, data acquisition and spacecraft bus interfacing are implemented with a mix of both hardware and software in this subsystem. This allows autonomous operation of the experiment with periodic data transfers to the spacecraft for storage and subsequent transmission to a ground facility. The experimental housing is a Naval Research Laboratory (NRL) built Standard Electronic Box (SEB) modified for four D

boards. The entire experiment package is to remain under an allotted weight limit of 5.5 lbs. The housing is divided into two compartments. The primary one houses the microprocessor board, the primary D boards and power conversion hardware. This compartment provides high density, aluminum shielding to internal electronics. The secondary compartment houses the D board containing two ferroelectric capacitor ICs which will be exposed to a higher total dose over the life of the experiment (planned for one year but three years will be attempted). The software subsystem controls all the I/O and housekeeping functions, provides the logic control necessary for the test routines and supervises the data acquisition on the D board subsystem. The code is written in "C" and resides in the microprocessor boards one-time programmable read only memory (PROM).

The two primary sets of experiments are fatigue and aging tests. During the fatigue test cycle, the devices are cycled with a bipolar drive signal and measurements are made at logarithmic decade cycles (i.e. 10^x, where x=1,2,...) and at least every 24 hours to give ground controllers at the mission control facility information on the status of the experiment.

The aging test measures the loss of the remanent polarization on a selected D board over a sequence of time intervals. The time interval for the FERRO experiment is

chosen every logarithmic decade from 10^0 to 10^4 seconds, followed by additional measurements every 24 hours. It is performed on one bank each of two D board ICs, one in the primary housing and one in the secondary housing. The devices are first connected to the Sawyer-Tower circuit for the test sequence, a "write" is performed on the bank to drive all devices to saturation, immediately following the individual set of ferroelectric capacitors or DUTs are switched to the "read" position and sequentially measured on the Sawyer-Tower circuit. Once all devices have been measured, both terminals are switched to ground and the devices are allowed to age.

After the aging tests are performed, the D bank is returned to the fatigue sequence. This battery of tests continues for 30 days. This sequence will allow several measurements of both the fatigue and aging response for each bank of capacitors over the experiment design life of one year.

C. PROPOSED STANDARDIZED TESTING METHOD

Steve Bernacki of Raytheon Equipment Division, under a US Army Strategic Defense Command (SDC) contract, spearheaded a Ferroelectric Memory Testing Team composed of various companies and defense laboratories. With the primary focus on discrete capacitor testing, a standardized testing procedure initiative was developed to allow direct, meaningful comparison of thin film capacitors fabricated and tested at

independent laboratories. The standard is simple to reproduce with industry, government and university equipment, and comprehensive enough to characterize those parameters relevant to SDC and other ferroelectric memory designs. A set of baseline parameters were agreed upon as a requirement for the testing procedures. This was the history and motivation behind the standardized ferroelectric capacitor testing method for nonvolatile semiconductor memory applications, presented and submitted to the IEEE for approval in March, 1992 [Ref. 44]. Some basic definitions are reviewed in Figure 3.7.

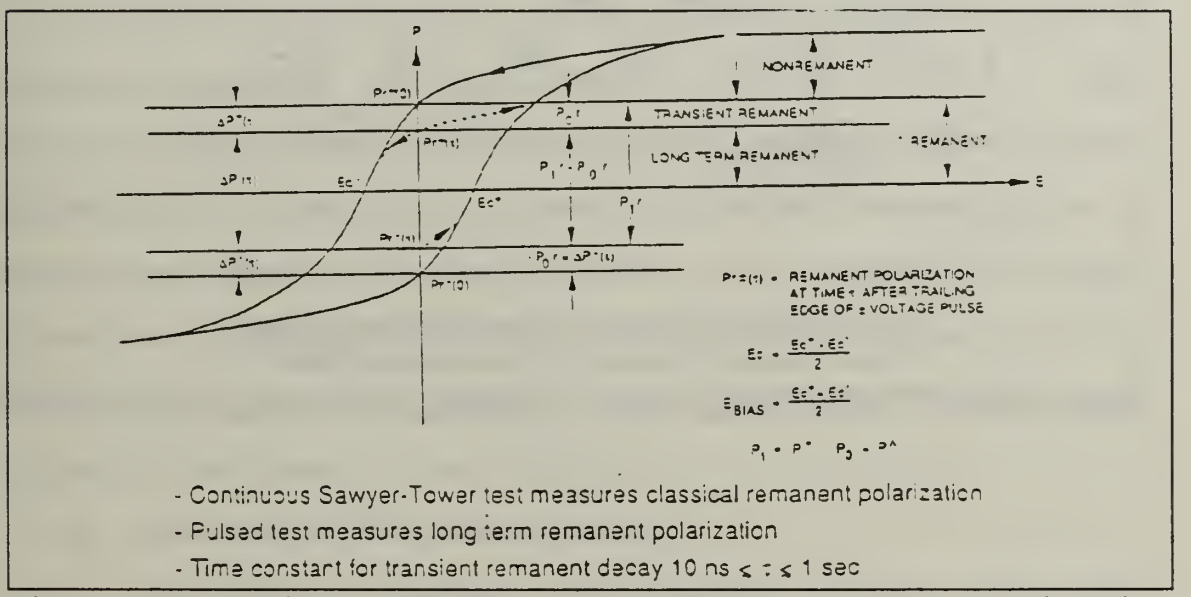


Figure 3.7: Time dependent, asymmetric, pulsed polarization definitions [Ref. 50].

The standardized testing procedure can be summarized into 15 major steps or items [Ref. 50]:

1. Five Pulse Wavetrain

A five pulse wavetrain, depicted in Figure 3.8, is the simplest waveform that probes the complete polarization hysteresis. It is basically a read-write test of the ferroelectric device for memory applications. For this test, it is acceptable to use a four pulse (+ + - -) if a 1 second read-write delay is maintained.

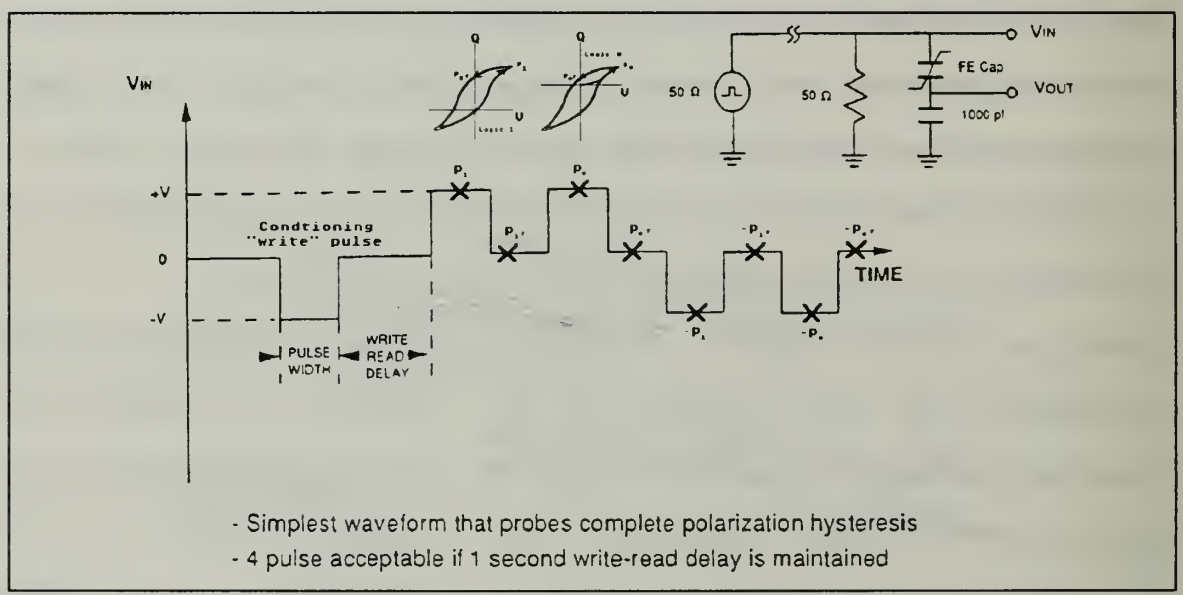


Figure 3.8: Five pulse PUND type wavetrain [Ref. 50]

2. 2, 3 and 5 Volt Measurement Voltage

As a minimum, perform all measurements at 2, 3 and 5 volt pulse amplitudes **in that order**, to avoid being affected by the "pumping up" effect. For comprehensive measurements, voltages from 1 to 5 volts in 0.5 volt increments and from 5 to 10 volts in 1 volt increments is recommended.

3. 100ns Pulse widths

Pulsed polarization decreases with decreasing write pulse width. Using 100ns or below is necessary for high speed memory design. Memory designs employ approximately 50ns write and read pulse widths. If there is a dependence on write pulse widths, 100ns is a more conservative value which will improve the chances of successful memory operation during the early stages of debugging and testing.

4. Read Pulse Rise Time

For test systems with adjustable rise times, set the rise time to the minimum value possible without causing ringing (overshoot and oscillations) in the circuit. This should be determined by measuring the voltage right on the ferroelectric capacitor by means of a second sensing probe or bond on the capacitor or bonding pad. For ordinary 50Ω output impedance pulse generators use what the generator puts out and identify the make and model. Good pulse generators have typical rise times of 5ns to 10ns.

5. One Second Write-Read Delay

In order to ensure measurement of only long term remanent polarization, standardize the write-read delay to one second to allow any transient remanent polarization to decay away. Most transient remanent polarization decays within 1ms for standard samples. One second is adequate for all tested films with a 100ns write pulse width. For consistency, also

set all interpulse delays to one second. This will avoid confusion in the five pulse test, for example, where each read pulse is simultaneously a write pulse for the next measurement.

6. Leading Edge of Read Pulse

Record data at the leading and trailing edge of the read pulse. The leading edge reduces time required for the reading operation. The trailing edge increases this signal to common mode ratio. A good guideline is 5 RC time constants after the beginning of the transition.

7. 50Ω Terminating Resistor

For pulse generator measurements use a 50Ω terminating resistor as close as possible to the capacitor; on the probe card for wafer measurements or on the end of the generator cable. Use a 0.5 Watt carbon composition resistor and measure it to make sure the value is 50 ± 1 Ω. This means that the pulse generator will have to deliver twice the open circuit output voltage as will be applied across the ferroelectric capacitor.

8. 40x40 μm Capacitor Size

The 50ns pulse width standard limits the capacitor size to less than 40x40 μm in size due to RC time constant considerations. Typical PZT capacitance and 50Ω source impedances yield RC≈4ns which will allow the voltage on the capacitor to achieve full value for at least 30ns of the 50ns

pulse width. Also, one should test as small a capacitor as possible to simulate actual memory conditions and increase the signal to noise ratio. Single 8x8 μm capacitors are preferred.

9. Capacitive Sensing Circuit

A capacitive charge sensing circuit should be used rather than a resistive current sensing circuit. Due to extremely short rise times, capacitive reactance dominates over real resistance in determining voltage levels and current flows, at least during the leading edge of the pulse, so a capacitive sense is a closer simulation. Current sensing is more difficult to perform accurately due to reflections, ringing, etc. Capacitive sensing can also be done with a lower bandwidth storage scope.

10. 470 or 1000 pf Sense Capacitor

For sensing 40x40 μm ferroelectric capacitors, use a 1000 pf sense capacitor. For smaller ferroelectric capacitors use 470 pf. The purpose of this specification is to standardize the reverse bias that is placed across the ferroelectric capacitor when the applied write or read pulse returns to zero, and there is still a charge, and hence a voltage, across the sense capacitor. This will tend to reverse the polarity of the ferroelectric capacitor if there are any domains with low coercive voltages in the reverse direction. The voltage can be minimized by the use of larger

sense capacitors but at the expense of detectable signal (Q=CV). Use a low loss capacitor with good high frequency characteristics such as a type NPO ceramic or a polystyrene capacitor.

11. Minimum sample size

Use a minimum sample size of five capacitors. This is necessary for statistically significant data. Always plot error bars representing $\pm\sigma$.

12. Single Sweep Waveforms

Use a single sweep waveform with a storage scope rather than applying a repetitive waveform to the capacitor. Again, due to the "pumping up" effect, a repetitive waveform will give erroneously optimistic values of polarization.

13. Preconditioning Procedure

Polarization depends on prior voltage history (poling). Therefore the preconditioning voltage should not exceed the measurement voltage. Precondition with repeated single test waveforms until stable. Five volts and below are relevant to semiconductor memory design.

14. Drive Bottom Electrode Positive

Raytheon has noticed a distinct polarity asymmetry in their capacitors. Their memory design drives the top electrode negative for reading which is equivalent to driving the bottom electrode positive on their patterned capacitors. Therefore repeating measurements with the leads reversed and

mapping the asymmetric pulsed polarization onto a continuous hysteresis curve can reveal polarity dependent transient remanent polarization.

15. Circulate a Calibration Standard

For team testing and comparison of data, a standard calibration sample should be circulated among all team members to compare different test stations and ensure uniformity of test results. Overall adherence to a set of standardized test procedures should allow direct comparison of test data generated at different facilities and independent confirmation of test data by potential users and designers.

IV DESIGN CONSIDERATIONS AND TEST SYSTEM DEVELOPMENT

A. PROPOSED NEW TEST SYSTEM DESIGN

The motivation behind designing a new test system is primarily to overcome current SMS limitations previously mentioned in Chapter III. Host PC dependence, and slow cycling speeds for fatigue tests were among the limitations specifically targeted. It is hoped that the proposed new test system design will be flexible enough to meet future demands in ferroelectric capacitor device testing. In light of the increased emphasis on testing ferroelectric devices for memory applications, every effort was made to maintain close adherence to the proposed standardized testing methods mentioned in Chapter III. The resulting design proposal will allow simple initial programming by the user through PC interface on any IBM compatible computer. The design also allows independent, autonomous operation after initial programming and the capability to digitally store test data measurements for subsequent analysis.

1. Overall System Design

The test system design consists of four individual and identical test boards. The test boards can be housed in a larger test box, hardened as necessary for possible future testing in a linear accelerator. The ferroelectric capacitors

designated for direct exposure could be jigged or placed on the outside of the box and different levels of shielding could be used for different test boards inside the box. Each test board can be represented by a block diagram shown in Appendix A (NPS THESIS: TEST SYSTEM DESIGN). Refer to Figure 4.1 below for the description of the test board.

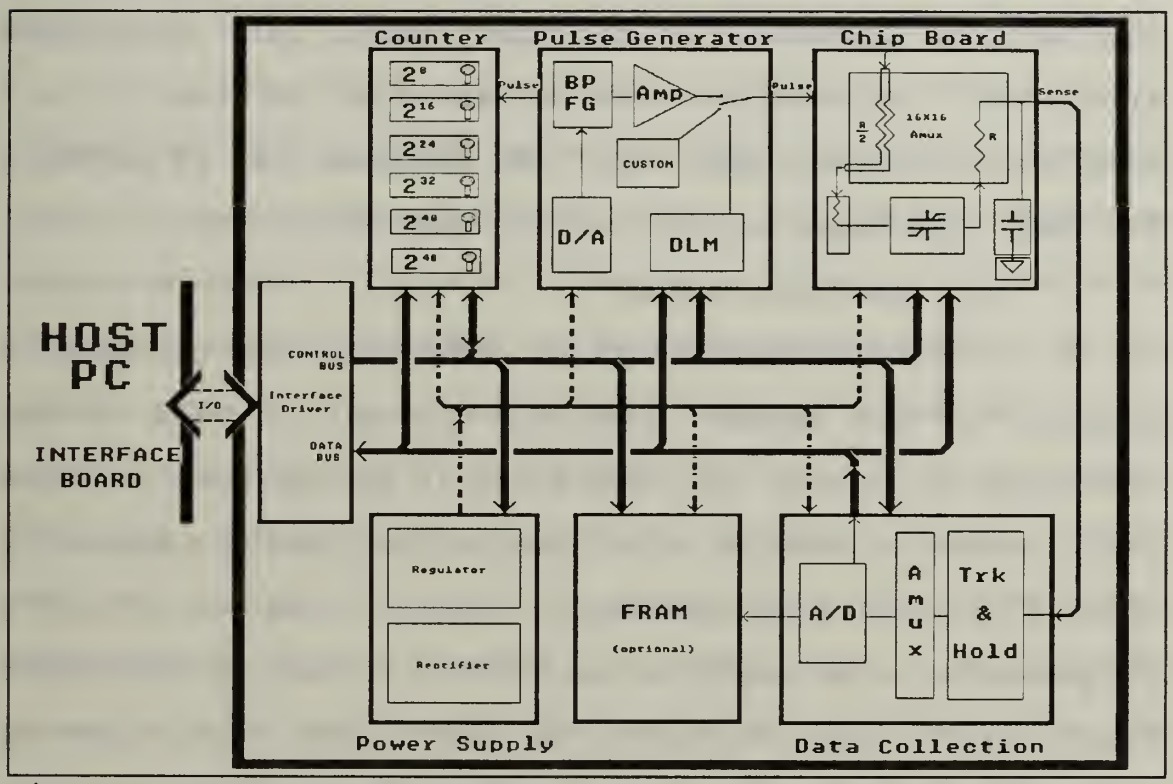


Figure 4.1: Block diagram of the Test Board and associated subsystems.

An interface board, located inside the host PC, is used for initial instruction loading to the Interface Driver subsystem, one located on each test board. The Interface Driver then generates the appropriate data, control and power supply bus signals for test board operation. The Pulse Generator subsystem, also located on each individual test board, takes

the data and control signals to generate an appropriate pulse for the Cycle Board and Counter subsystems. The Counter subsystem signals the user when a predetermined number of cycles are complete. The ferroelectric capacitors are normally located on the cycle board in the Cycle Board subsystem and after cycling they generate the data that is sampled and processed by the test board Data Collection subsystem. The data can then be stored on the host PC hard disk drive or on a floppy disk. An itemized list of hardware for each test board is provided in Appendix B.

a. Interface Driver

The Interface Driver schematic can be seen in Appendix A (NPS THESIS: INTERFACE DRIVER). There is one Interface Driver per test board and it allows user selected test boards to receive data, control and pulse signals by using a test board identification system. This consists of a programmable array logic device (PAL) which allows the active board select (BS*) signal to be sent if the test board is selected. The logic consists of a programmed EO310 PAL to emulate four AND logic gates which look for a test board match and consequently activates one OR logic gate feeding a D-flip flop which generates the BS* signal. Tri-state buffers are used to hold the proper control signals.

b. Pulse Generation Subsystem

The Pulse Generation subsystem schematic can be seen in Appendix A (NPS THESIS: PULSE GENERATOR). There is one Pulse Generation subsystem per test board and it receives the data and control bus signals necessary from the Interface Driver to generate the proper waveform for the Cycle Board subsystem.

The Pulse Generation subsystem consists of a Digital to Analog (D/A) converter which feeds an on-board voltage controlled oscillator (VCO) or bipolar function generator (BPFG). Several inexpensive VCOs with desirable frequency ranges of 100kHz up to 20MHz are currently on the market, but few generate a fast bipolar (plus and minus square) waveform that is required for proper ferroelectric capacitor cycling (see Chapter V, Hardware Tests). Most generate a positive pulse of equal pulse width and pulse interval and with a limited frequency range. A function generator on a chip can be controlled by a D/A converter and it can generate sinusoidal, sawtooth, and even square waveforms but it is difficult to find a BPFG with a large enough frequency range (see Chapter V, Hardware Tests).

When the proper waveform is generated by the VCO/BPFG, the amplitude has to be controlled or amplified. For fast cycling, an amplifier with a high slew rate must be used. The Harris HA-2540 operational amplifier was selected due to its very high slew rate of 400 V/μs. This yields a

25ns rise time for a 10 V pulse. The ability for the user to select the proper magnitude of the waveform via software should also be incorporated. The initial design attempted to use a magnitude D/A converter feeding a voltage controlled resistor (VCR) used in the feedback of the fast slewing operational amplifier (FSOA) to control the gain (see Chapter V, HA-2540 Tests). Failure of the VCR tests led to substituting a set of individually selectable resistors (16) in the FSOA feedback loop. By using two 8x1 analog multiplexers for selection control, 80 different resistance combinations are possible. With proper resistor value selections, a wide range of software controlled resistance is possible and adding a potentiometer in series allows for fine tuning of resistance values in the FSOA feedback loop.

Due to fixed hardware limitations, the VCO or BPFG is an area in the design that can limit the frequency range and shape of the pulse generated to cycle the test chip. To make the design more flexible, a "custom" waveform input is provided. This allows the user to bypass the test board waveform generator and use any external waveform generator, portable or otherwise, for selection by the pulse select analog multiplexer at the output of the Pulse Generator subsystem. Also available for selection are the "five pulse wave trains" of varying amplitudes (±2,±3,±5 and an extra bonus ±7 V). The five pulse wave trains are part of the

proposed standardized testing methodology for memory applications mentioned in Chapter III-C-2.

c. Cycle Board Subsystem

The Cycle Board subsystem schematic can be seen in Appendix A (NPS THESIS: CYCLE BOARD). It consists of eight individual and identical Chip Sets (see Appendix A, NPS THESIS: GENERIC CHIP SET). Each Chip Set is capable of cycling or providing specific pulse wavetrains to one set of on-chip ferroelectric capacitors. The Chip Set also contains the sense capacitors required for the Sawyer-Tower testing circuit and the proper analog switch to ground. The Chip Set then provides the output measurements for the Sample, or more appropriately, the Track and Hold part of the Data Collection subsystem.

The heart of the Chip Set, and of the over-all test system design, is the Analog Device AD75019 16x16 analog crosspoint multiplexer seen in Figure 4.2. The AD75019 provides the analog switching necessary to create the Sawyer-Tower testing circuit for the on-chip ferroelectric capacitor. It eliminates the need for all large, real estate extensive sense capacitors normally required for each ferroelectric capacitor being tested by the system, except for seven shared by all ferroelectric capacitors. Seven were used due to the largest set used by National Semiconductor's on-chip ferroelectric capacitor design (see Appendix C: National

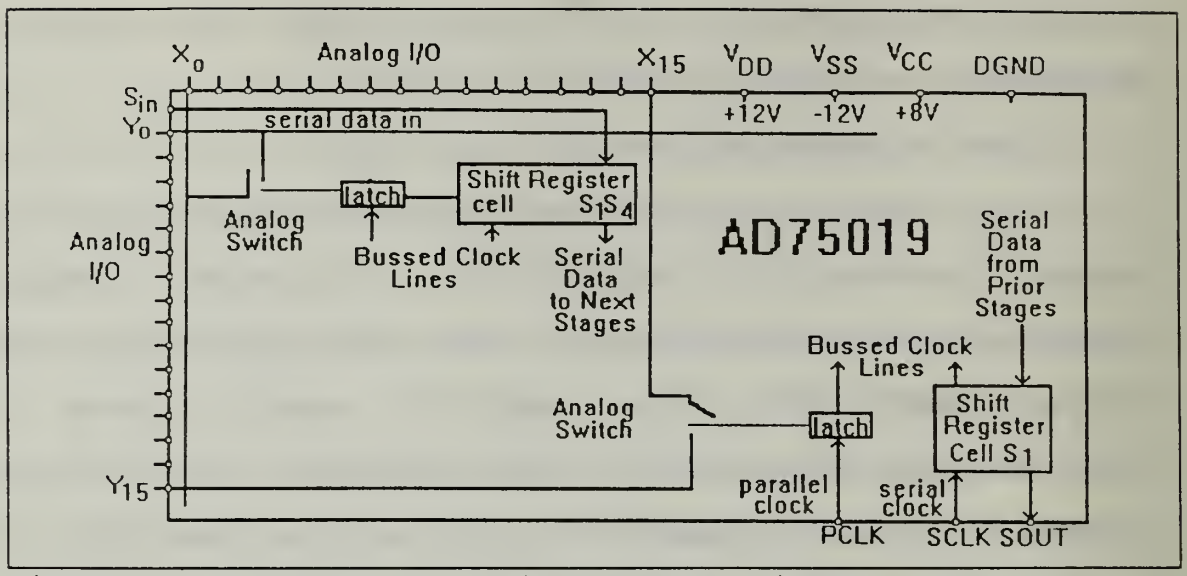


Figure 4.2: AD75019 Functional Block Diagram [Ref. 51]

Semiconductor Chip Pin-out). There are 256 bi-directional CMOS analog switches available in a 16x16 array with a typical low on-resistance of 150Ω. The AD75019 connects any or all of its 16 analog inputs (X for this design) to any of its 16 analog outputs (Y for this design). Data to set up the analog switches (DATA IN) is loaded serially via the signal input (SIN) and clocked into an on-board 256-bit shift register via a serial clock (SCLK). When all of the switch settings are programmed, data is transferred into a set of 256 latches via a parallel clock (PCLK). The serial shift register is dynamic, so there is a minimum clock rate of 20kHz. The maximum clock rate of 5MHz allows loading times as short as 52μs. The switch control latches are static and will hold their data as long as power is applied. Power is specified at ±12 V and at ±5 V, but the supply voltage span can be as little as 9V or up to 26V. A power supply of ±10 V and +5 V

meets test system design requirements to allow pulse signals of up to ±10 V to be used. Also considered for design was Mitels MT8816 8x16 crosspoint multiplexer with a lower on-resistance, but it operates at smaller supply voltages. GoldStar, Motorola, Raytheon, RCA/Harris and Silicon Systems also make smaller arrays with lower voltage limits. Sierra makes a larger switch (32x32) for unidirectional 5-volt logic signals only.

The generic Chip Set design allows for testing of existing National Semiconductor on-chip ferroelectric capacitors (see Appendix A, NPS THESIS: NC CHIP SET (DEMO)). To allow testing of any other on-chip ferroelectric device, a jig extension was incorporated into the design. This adds flexibility and only requires a simple adapter to meet a specific chip pin-out. A control software library for specific devices could be written as new on-chip devices are considered for testing. An example is an adapter cable for a Ramtron on-chip ferroelectric capacitor set (see Appendix C: Ramtron Chip Pin-out) as seen in Appendix A (NPS THESIS: RAMTRON CHIP ADAPTER).

Output lines are connected to the sense bus which go to the Sample and Hold part of the Data Collection subsystem. A final note: care must be taken to ensure the sense bus lines from each individual chip set are of equal length. This is to ensure equal resistance when the signal reaches the Data Collection subsystem.

d. Counter Subsystem

The Counter subsystem schematic can be seen in Appendix A (NPS THESIS: COUNTER). It consists of six 8-bit down counters and associated logic to allow data collection at a predetermined number of cycles. A buffered Pulse signal drives the six counter clocks (CCLK) which count down from a user determined number of cycles, giving a visual light indication of counter status to the user and eventually yielding a counter done (CNT DONE) signal. With six 8-bit counters, 2^{48} or about 2.8×10^{14} cycles can be counted. This provides an ample number of cycles for fatigue testing of ferroelectric capacitors. The only limitation is the cycling frequency and therefore how long it will take to get to 2^{48} cycles. The SMS could only cycle at 180kHz due to design limitations. With a proposed high speed cycling frequency of 4MHz for the new test system, more timely fatigue test results are possible. Taking the cycling frequency even higher to the theoretical maximum of 1GHz dramatically decreases the amount of time required to conduct fatigue tests as shown in Table I. Note that with six 8-bit counters in the design, 2^{48} or about 2.8×10^{14} cycles are the maximum number of cycles that can be counted.

Table I CYCLE TIME AS A FUNCTION OF CYCLING FREQUENCY

Frequency	10^{11} Cycles	10^{13} Cycles	2^{48} Cycles
180 kHz	6.43 days	643 days	49.55 years
500 kHz	2.31 days	231 days	17.84 years
1 MHz	27.8 hours	115.7 days	8.92 years
2 MHz	13.9 hours	57.8 days	4.56 years
4 MHz	6.95 hours	28.9 days	814.5 days
1 GHz	100 sec	2.78 hours	3.26 days

e. Data Collection Subsystem

The Data Collection subsystem schematic can be seen in Appendix A (NPS THESIS: DATA COLLECTION). The Data Collection subsystem incorporates the analog switch to ground used with the sense capacitors and sense bus. The analog switch to ground consists of two sets of quad analog JFET switches, controlled by a control bus signal. This allows the proper sense capacitor measurement to be isolated and sent via the sense bus to the Sample and Hold circuit (see Appendix A, NPS THESIS: SAMPLE & HOLD).

Using a fast Analog Device built HTS0300 track and hold device gives an added improvement over the SMS sample and hold and allows for measurements using faster cycling speeds and shorter pulse lengths. For example, the 100ns pulse width wavetrain recommended in the proposed standardized testing

method mentioned in Chapter III is now possible with the new design. Sample A (SA) corresponds to the pulse sample ($\pm P_1$ or $\pm P_0$) and sample B (SB) corresponds to the remanent sample ($\pm P_{1r}$ or $\pm P_{0r}$) as shown in Figure 3.8. A delay line machine (DLM), represented in Appendix A (NPS THESIS: DELAY LINE MACHINE), is used to generate proper pulse widths and timing sequence, depicted in Figure 4.3, for measurement.

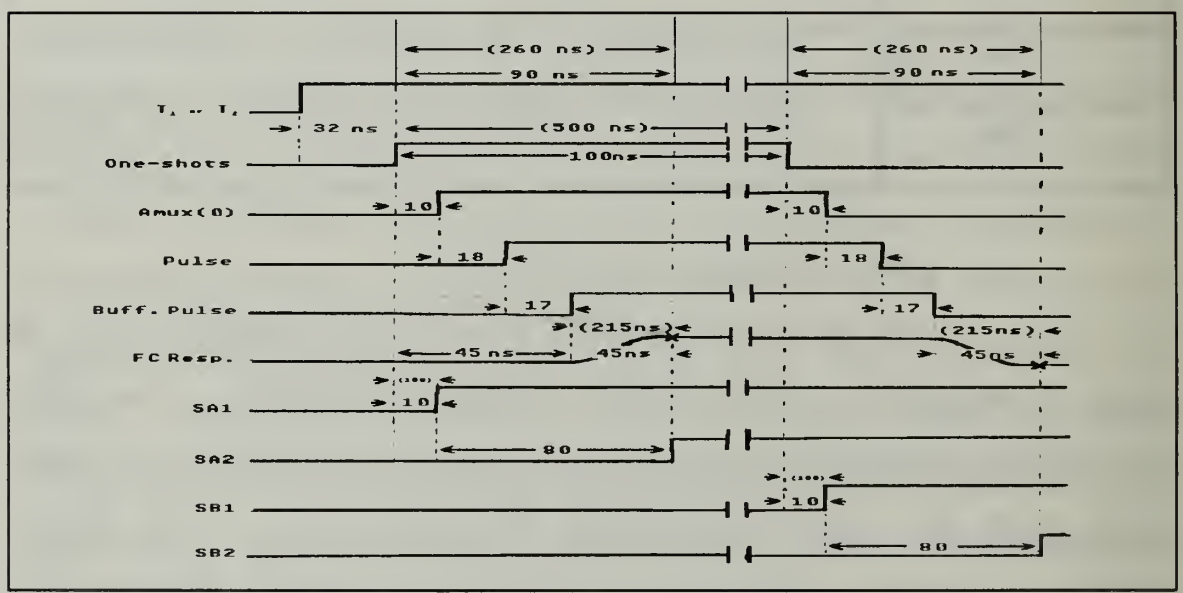


Figure 4.3: Timing Diagram for DLM one-shots and corresponding Sample signals.

The DLM consists of two sets of one-shots, one fast to generate 100ns pulse widths and one slow for 500ns pulse widths. The one-shots also trigger the SA and SB signal at the proper time, and select the pulse test wavetrain via a AMUX(0) signal to the pulse select analog multiplexer at the output of the Pulse Generator subsystem.Due to design limitations (see Chapter V, AD75019 Test and Calculations),

only ferroelectric capacitors with capacitance less than 60 pF can be used for the 100ns pulse test. Larger capacitors of capacitance less than 270 pF must use the 500ns pulse widths.

The proper measurement is sent via a 16x1 analog multiplexer and buffers to an analog to digital (A/D) converter. The digital data is then sent via the data bus to the host computer for hard disk or floppy disk memory storage. One could even place a FRAM on the test board as a back-up to store data when power fails or host computer difficulty is encountered during the data storage phase.

f. Power Supply

The power supply must be capable of meeting the demands of the test board circuitry and its operation when fully loaded with maximum size ferroelectric capacitors. The simplest design consists of on-board rectifiers and regulators to enable the test system to operate from conventional AC electrical outlets. Simpler yet is direct feed from an external ±15 V DC power source, using resistors to voltage divide the ±15 V for every DC value needed on the test board.

V EVALUATION AND RECOMMENDATIONS

A. HARDWARE EVALUATION

1. AD75019 Analog Crosspoint Multiplexer

Since the AD75019 Analog Crosspoint Multiplexer is a key component in the new test system design, the test set up depicted in Figure 5.1 was constructed to closely simulate how the AD75019 will typically operate and to view any distortions or delays involved with the internal connections.

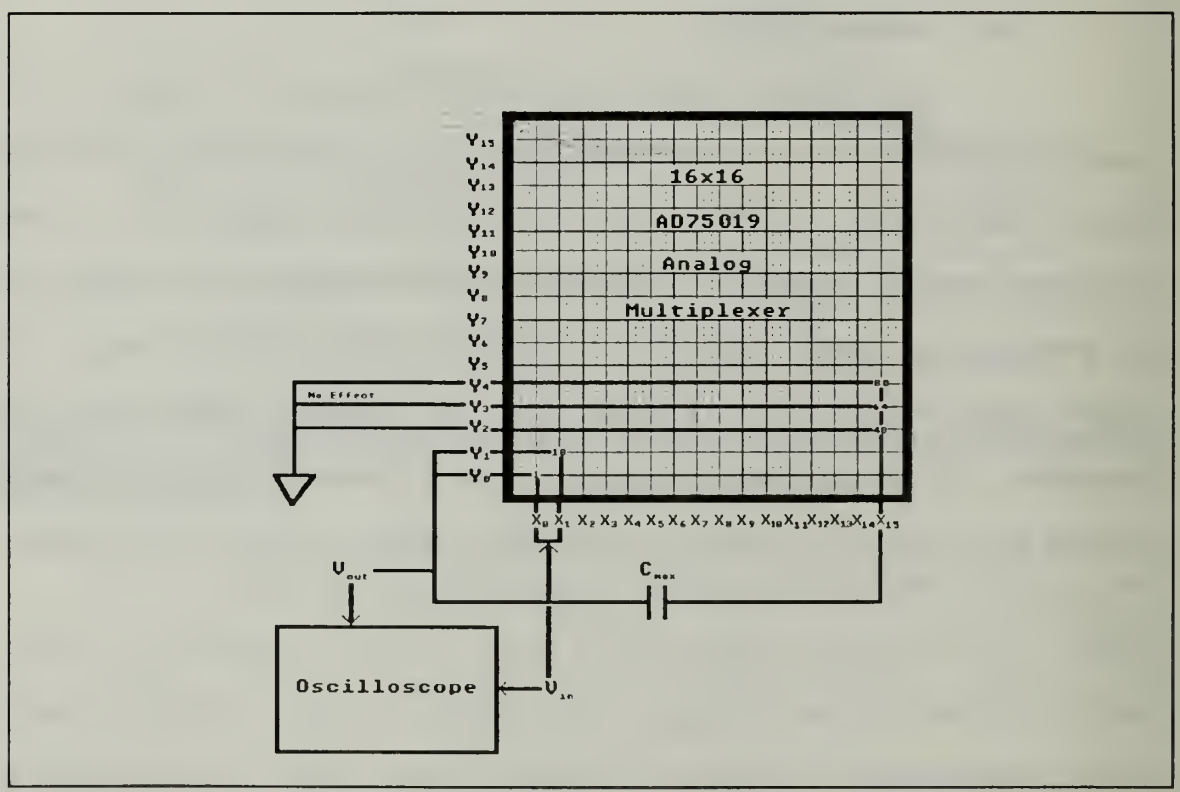


Figure 5.1: AD75019 Test Configuration.

In this configuration, proper loading of the AD75019 and corresponding analog switch connections were checked. Also,

the actual resistance through the device was measured. Using an 8086 IBM and an existing 82C55A Programmable Peripheral Interface Board (PPIB), a machine language program (TEST.COM, see Appendix D) written with Debug (IBM DOS 3.3) was used to send the proper loading sequence of bits to the AD75019. The PPIB consisted of ports A (address 300 hex, bits 1-8), B (address 301 hex, bits 23-40, all ground), C (address 302 hex, bits 9-12 and 13-16, serial data) and D (address 303 hex, control signal command 80 hex). Bit one of port A was used to send the SCLK pulses needed to load 256-bits to the shift registers of the AD75019. Bit two of port A was used for the PCLK pulse to load the data from the shift registers to the 256 latches of the AD75019. The serial data was fed to SIN of the AD75019 via a nested loop. A Wavetech generator provided a 4MHz square wave to check proper X (input) to Y (output) analog switch configuration of the AD75019.

To use the AD75019 for the Sawyer-Tower configuration involves routing the input waveform through the device and to the ferroelectric capacitor and then through the device once again to ground or to a sense capacitor (see Figure 5.2). This yields a combined theoretical resistance of 300Ω, which raises the RC time constant for a particular size capacitor. When conducting the "five pulse wavetrain" test discussed in Chapters III and IV, the 100ns pulse can only be used on ferroelectric capacitors of small capacitance due to the fast rise time required (approximately 5RC). This becomes crucial

for the timing considerations of the DLM design. Increasing the resistance slows down the rise time of the ferroelectric capacitor even further. The actual internal resistance measured from one X to Y connection of the AD75019 was an average of 126Ω. To lower the resistance of a signal through the device and therefore lower the RC time constant of a capacitor connected in series at the output, the signal in was run through the device in parallel using the two inputs X_o and X_1 and two outputs Y_o and Y_1 (see Figure 5.1). This should yield an internal resistance in theory of 126Ω/2 or 63Ω. An average resistance of 69Ω was actually measured. Optimal use of the number of X inputs and Y outputs available allows for two parallel signal routes, one for DUT1 and one for DUT2 (see Appendix A, NPS THESIS: NC CHIP SET (DEMO) and Figure 5.2). Using more than one route to ground (i.e. using Y_3 and Y_4) had no effect in lowering the combined internal resistance through the AD75019 for the pulse test configuration. Adding 69Ω for the first time through the device and 126Ω for the second time through to ground yields 195Ω or 200Ω for calculations.

The capacitor, C_{max}, used for the test configuration in Figure 5.1 represents the combined series capacitance

$$C_{max} = \left(\frac{1}{C_F} + \frac{1}{C_s}\right)^{-1} = \frac{C_F C_s}{C_F + C_s} \qquad (10)$$

where C_F is the ferroelectric capacitor, and C_s the large sense capacitor (see Figure 5.2). Using a rule of thumb of $C_s=4 \cdot C_F$, [Ref. 40], and substituting into equation (10) yields

$$C_{max} = \frac{4C_F^2}{5C_F} = 0.8C_F \tag{11}$$

Assuming the resistance, R, of the AD75019 is 200Ω, a rise time, t_{rise}, equal to $5 \cdot R \cdot C_{max}$, and a track and hold window of 40ns is used, for a 100ns pulse the maximum delay due to the track and hold window is 100ns - 40ns = 60ns before the SA1 pulse. The theoretical delay of the DLM is 45ns which is the minimum t_{rise}. This yields

$$45ns = 5 \cdot 200\Omega \cdot C_{max} \text{ -----} \rightarrow C_{max} = 45pF \tag{12}$$

Since $C_{max} = 0.8 \cdot C_F$ you can calculate C_F = 56.25 pF which is the theoretically largest capacitance of the ferroelectric capacitor that should be used. We also know that $C_s = 4 \cdot C_F$ = 225 pF. Similar calculations for a 500ns pulse and theoretical DLM delay of 215ns yields C_{max} = 215 pF, a maximum C_F = 268.75 pF ferroelectric capacitance that should be used for 500ns pulse tests, and corresponding C_s = 1075 pF.

The AD75019 was also checked for proper operation in the Sawyer-Tower mode with DUT1 and then with DUT2 connected

to a bank of seven sense capacitors. One unexplained anomaly did occur with the testing of the AD75019 when loaded for simultaneous cycling of the two DUT configuration (see Figure 5.2), the voltage feeding DUT1 was an order of magnitude larger than DUT2.

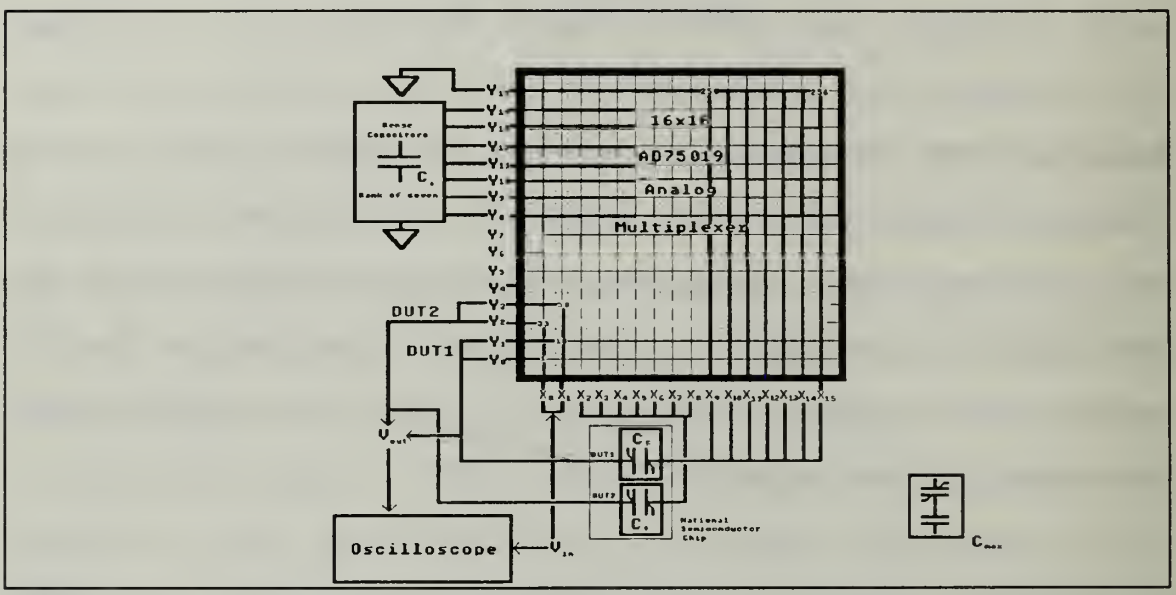


Figure 5.2: Two DUT test configuration of the AD75019 for simultaneous cycling.

This added load to DUT2 is either an internal problem to the AD75019 that has to be reported to Analog Devices or there is a problem with DUT2 on the ferroelectric capacitor chip. By reason, when DUT1 and DUT2 are wired together for cycling, the voltages should all be equal. Also, the AD75019 static registers displayed volatility by not holding their values unless the PCLK control line is kept low. A simple solution is to ensure PCLK is kept low during cycling and to periodically observe the hysteresis curve of the DUT to validate the AD75019 register contents. Finally, the fast 8x1

analog multiplexer that feeds the AD75019 is limited to ±6 V. This requires the use of a HA-2540 buffer operational amplifier with a fixed gain of two and then setting the inputs to half of the original ±2, ±3, ±5 and ±7 V at the magnitude analog multiplexer (see Appendix A).

2. HA-2540 Operational Amplifier

The Harris HA-2540 is a wideband, fast settling monolithic operational amplifier with a very high slew rate of 400 V/μm [Ref. 54: pp. 3-75-86]. Due to the high speed cycling frequencies anticipated for the test system, the fast slew rate and settling time of the HA-2540 is required to adequately control the magnitude and shape of the pulse used to cycle the ferroelectric capacitors. The original design approach for automatic gain control (AGC) of the HA-2540, and consequently automatic amplitude control of a pulse generated by an on-board function generator, considered the use of a voltage controlled resistor (VCR) in the feedback loop of the amplifier (see figure 5.3).

The principle is based on the characteristics of a n-channel JFET when used with a controllable (via software and a D/A converter) gate-to-source voltage, V_{gs} [Ref. 56]. The JFET has one *pn* junction, the gate-to-channel junction. For small V_{gs} values, there is a narrow depletion region and a current, I_d, will flow in the channel. As V_{gs} is made negative, the depletion region widens and the channel narrows.

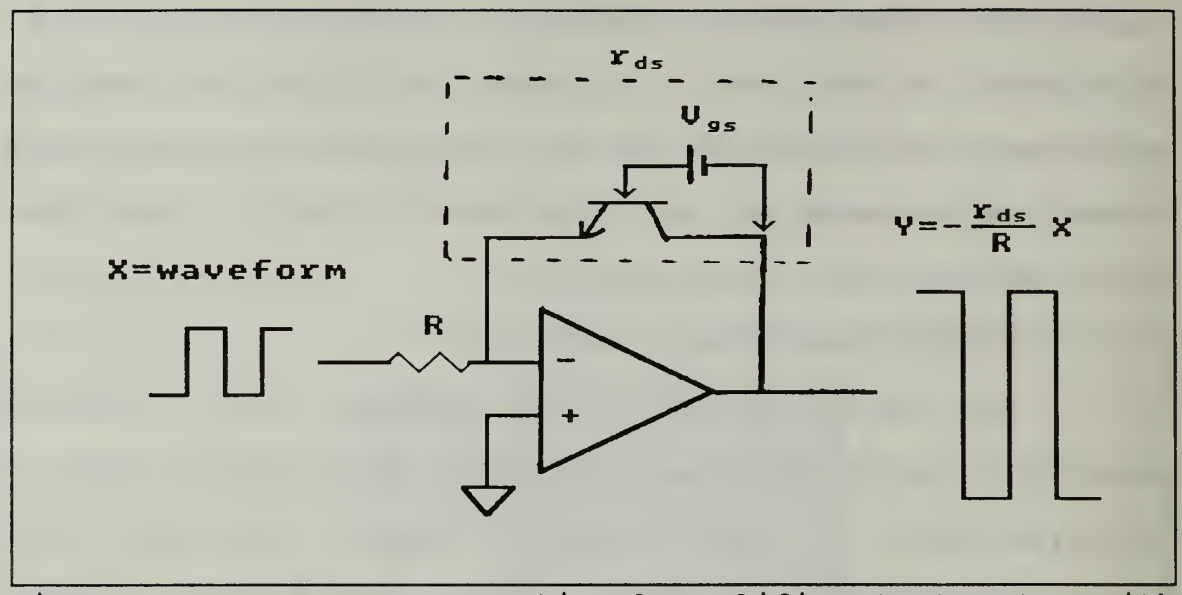


Figure 5.3: HA-2540 Operational Amplifier test setup with Voltage Control Resistor (VCR) JFET in feedback.

The narrowing of the channel causes its resistance to increase and therefore reduces the current flow, I_d, through it. The value of I_d is determined by the value of the drain-to-source voltage, V_{ds}, and the channel resistance, r_{ds}. For small V_{ds}, the JFET channel acts as a linear resistance whose value is controlled by the voltage V_{gs}. However, this region of operation of the JFET is not useful for linear-amplifier applications, as testing results indicate, due to the one-way resistance effect. For a bipolar (i.e. positive and negative square wave) pulse train, the JFET allowed only positive or negative values, depending on drain or source orientation, to pass through. For example, in the orientation shown in Figure 5.3, only positive Y values could be realized due to the JFET acting like a resistor for positive X values and like an open

circuit for negative X values. Amplitude control could only be accomplished for positive or negative pulses. Various configurations were attempted including two JFETs back to back to try to overcome the one-way resistance effect. Also attempted was fixing the gain (i.e. Y=5X) and then controlling the magnitude of the Y wave by operating the HA-2540 in saturation and adjusting the rail values with two D/A converters, one for positive and one for negative rail values. The operational amplifier was not really meant to operate this way and subsequent overheating problems supported test conclusions. It was then decided that the current design proposal would be most easily realized. The VCR in the feedback loop would be controlled via software and analog switches. There would be no need for a D/A converter to be used for the VCR in the feedback loop and subsequent AGC.

B. RECOMMENDATIONS

1. DLM

The ideal DLM would be an extremely fast programmable counter, capable of at least a 10ns delay between counts. The counter would eliminate the use of the one shots, D-flip flops and associated logic gates of the current DLM design. Since actual test of a 54HC4538 one-shot revealed a 140ns minimum pulse width possible vice the 100ns indicated in the specifications, it degraded the five pulse wavetrain test. Also, since the supposedly slow D-flip flop had a 55ns delay

vice the 80ns indicated in the specifications, the timing of the rising edge of SA2 (see Figure 4.3) and consequently the sampling of the ferroelectric capacitor occurs before the proper rise time is finished. Finally, the analog switch to ground LF13201 used in the SMS takes 500ns to open. This is not acceptable for the pulse testing so a 500ns delay at T1 and T2, before the one-shots, could be added or a faster switch could be used. The CD4066 has a typical delay of 60ns but it is normally open so the signal from the DLM has to be inverted prior to use.

Different parts mean different characteristic delays and this can change through usage and age of the parts. Therefore the current DLM design is extremely hardware sensitive. A fast programmable counter however could be used to generate 50ns, 100ns and any other width of pulse and send a SA2 sample signal at the proper rise time for the capacitance value.

2. Chip Reduction

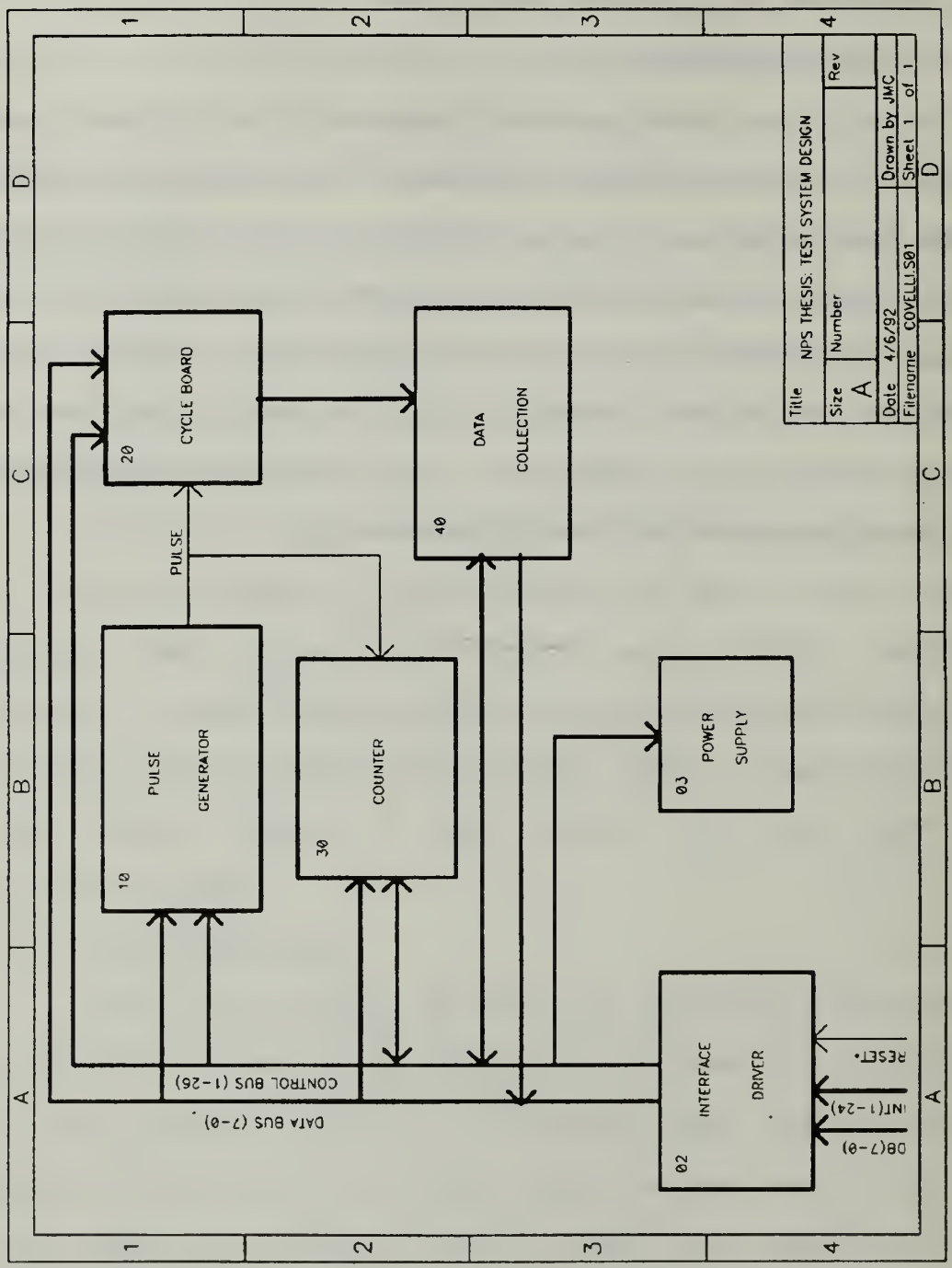
Since this design is based on hardware developed in the last two to five years, with the exception of the AD75019, there are probably chips on the market that are capable of taking the place of two or more chips in the current design. A chip reduction analysis would reduce the amount of real estate used and possibly make software programming easier.

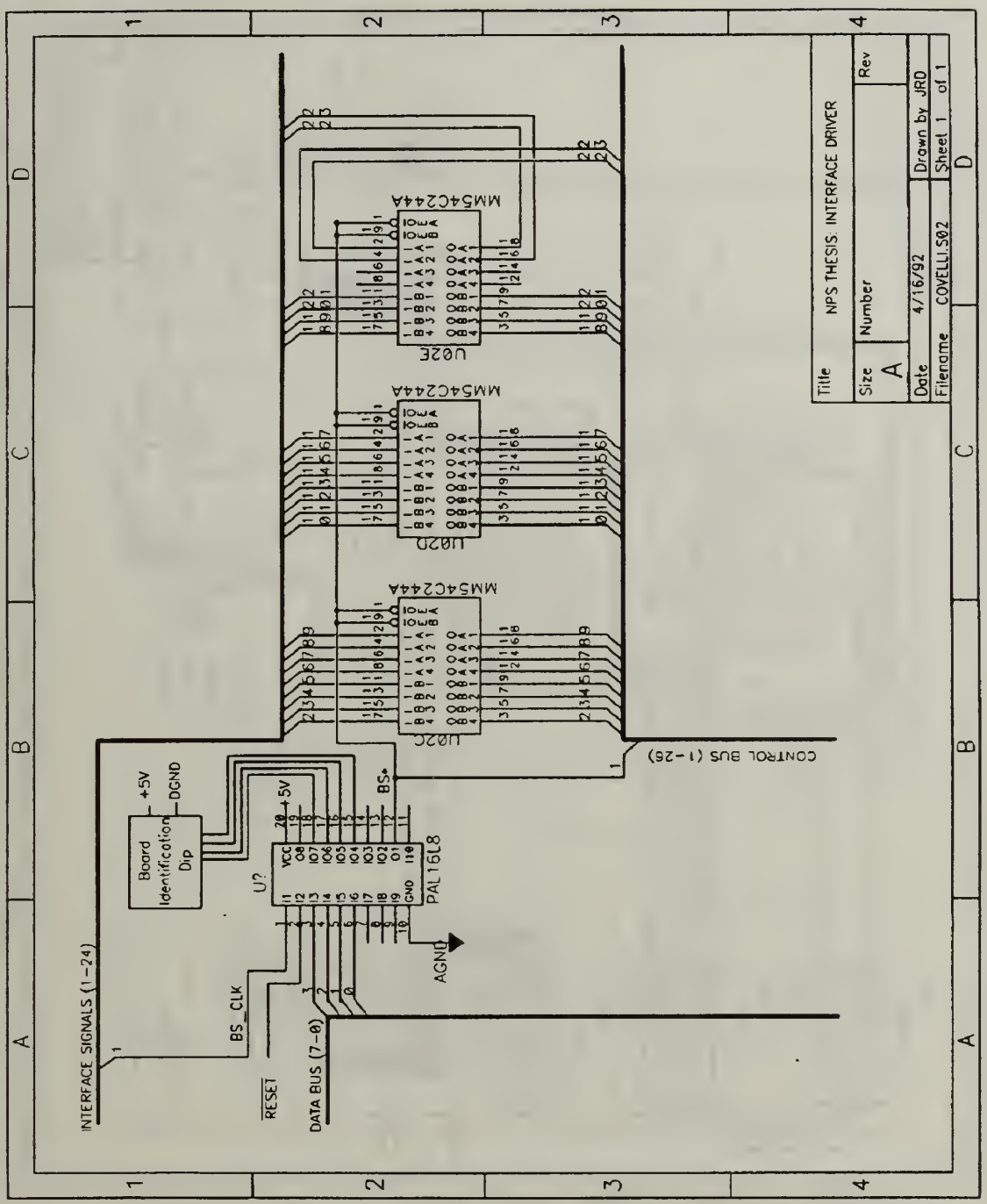
Software development should begin after such an analysis and when hardware requirements are firm.

3. Ordering Parts

It takes from six to twelve months to order parts through the normal supply system. Open purchase request speeds things up but it still requires a great deal of time to obtain necessary hardware. Once key components are available, testing them individually and on a finished prototype also requires more time. Therefore, it is very important that system hardware is identified quickly so the ordering and purchasing process can be initiated early.

APPENDIX A
NPS THESIS: TEST SYSTEM DESIGN (COVELLI.S01)

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INTERFACE SIGNALS (1-24)
Board Identification Dip
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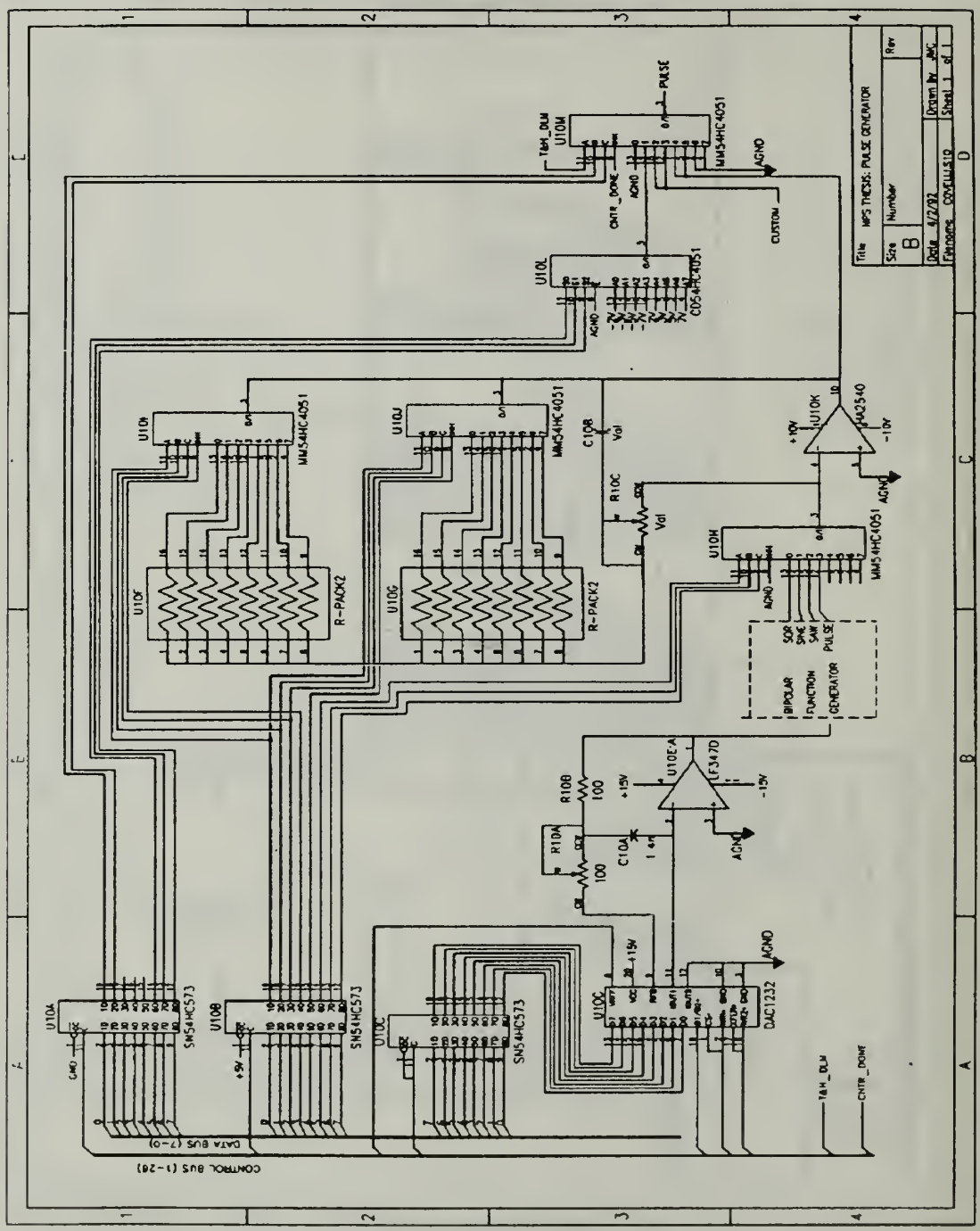
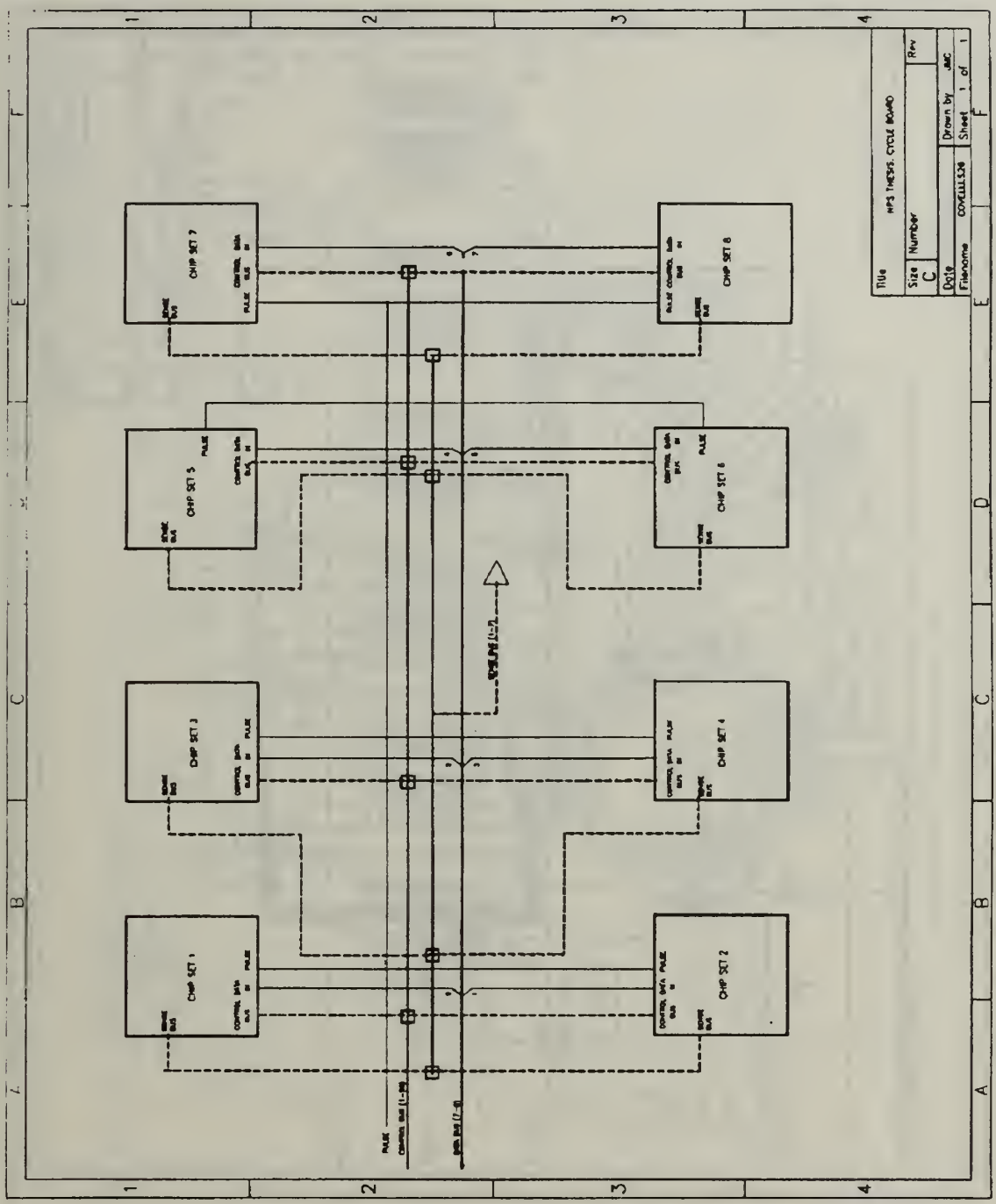
DGND
U?
PAL16L8
BS*
BS_CLK
RESET
DATA BUS (7-0)
AGND

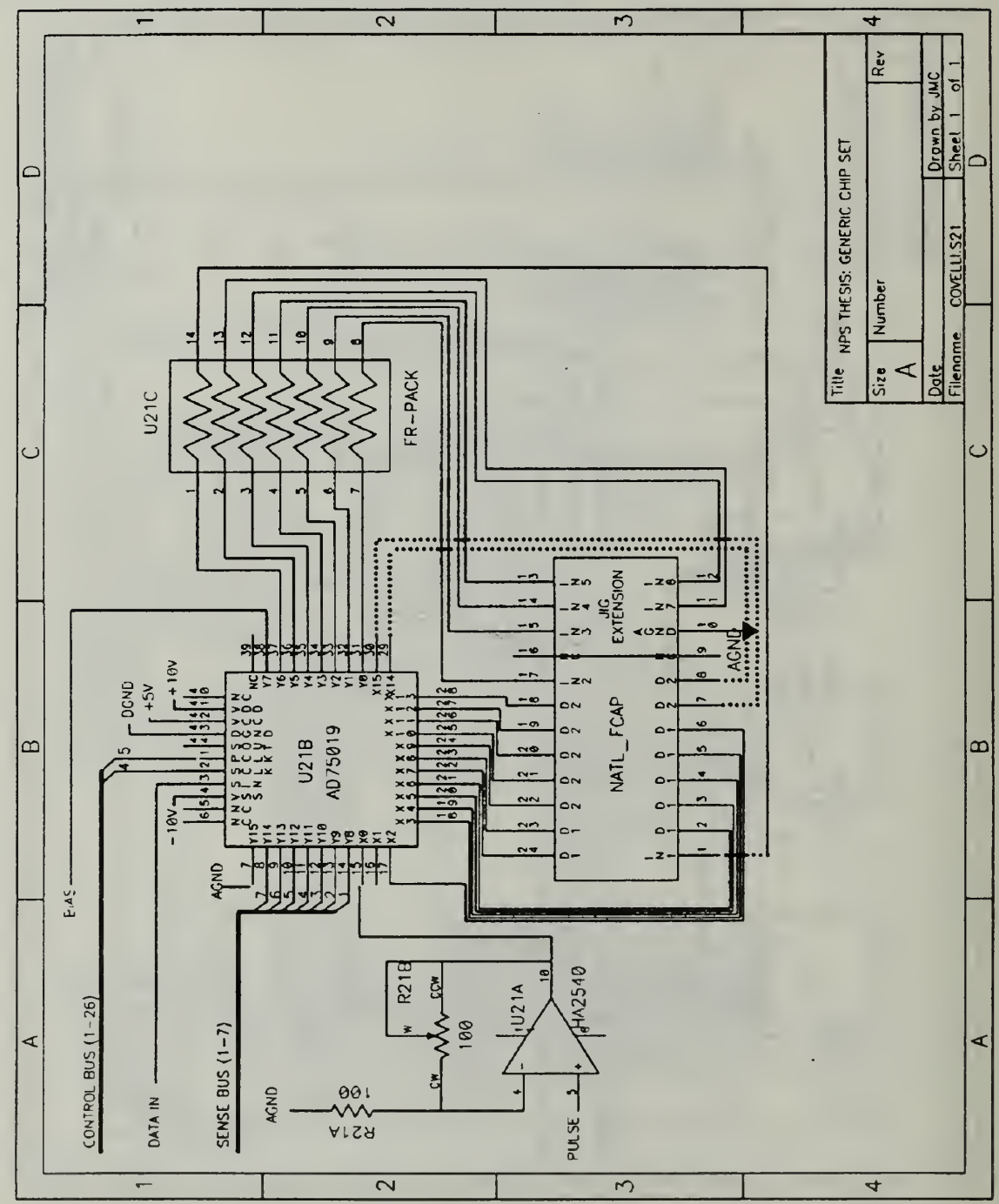
NPS THESIS: PULSE GENERATOR (COVELLI.S10)



NPS THESIS: CYCLE BOARD (COVELLI.S20)



NPS THESIS: GENERIC CHIP SET (COVELLI.S21)



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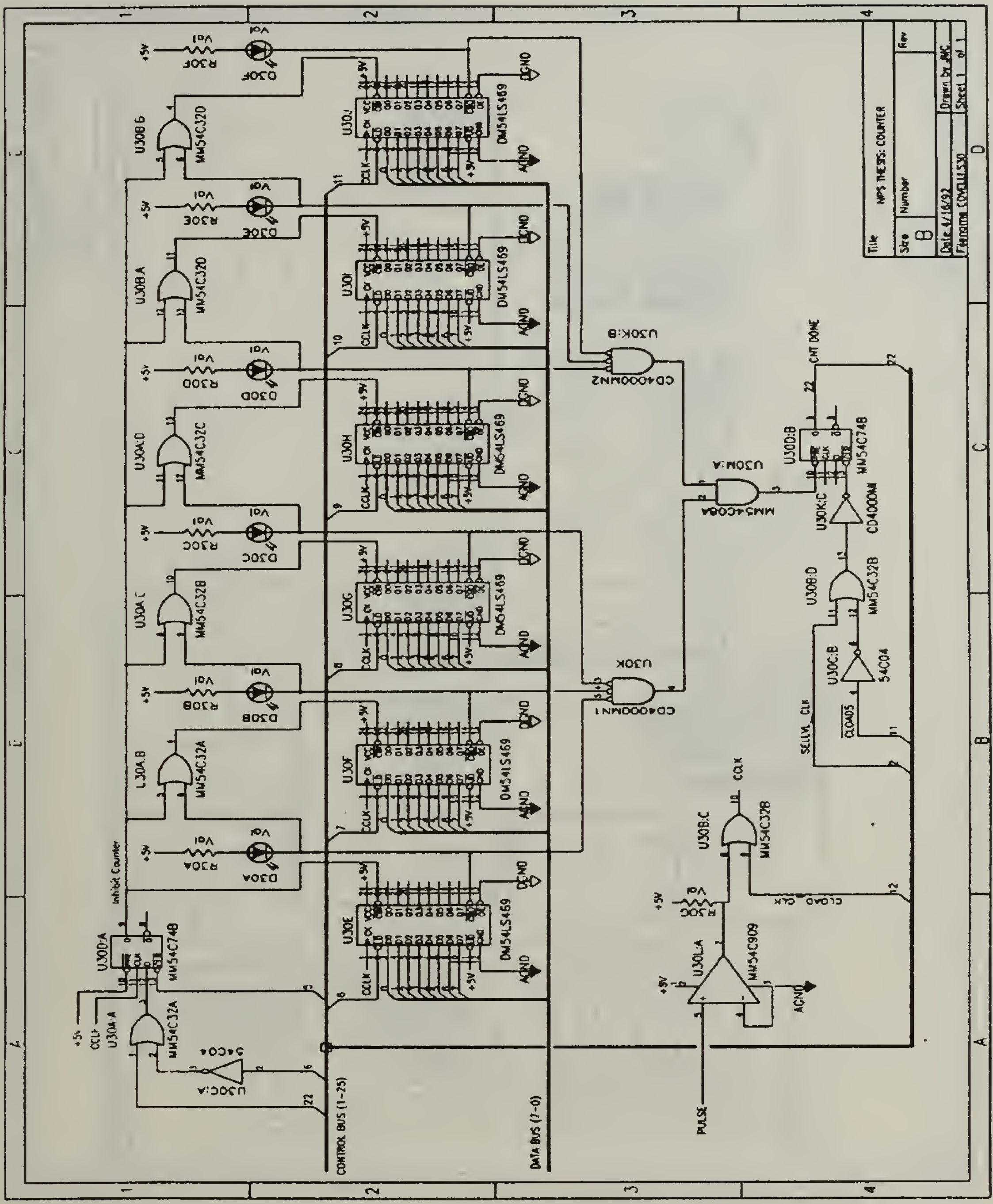

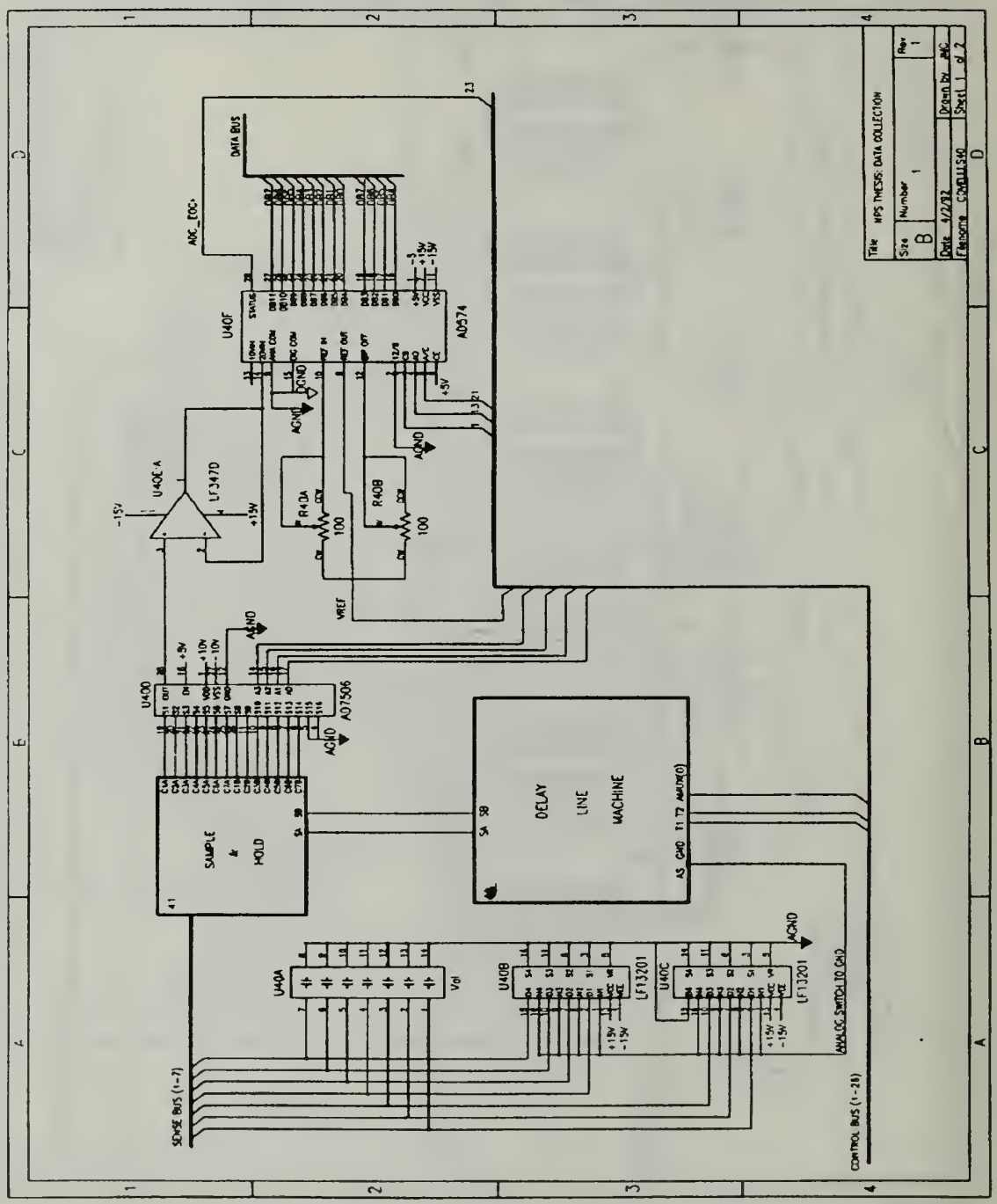
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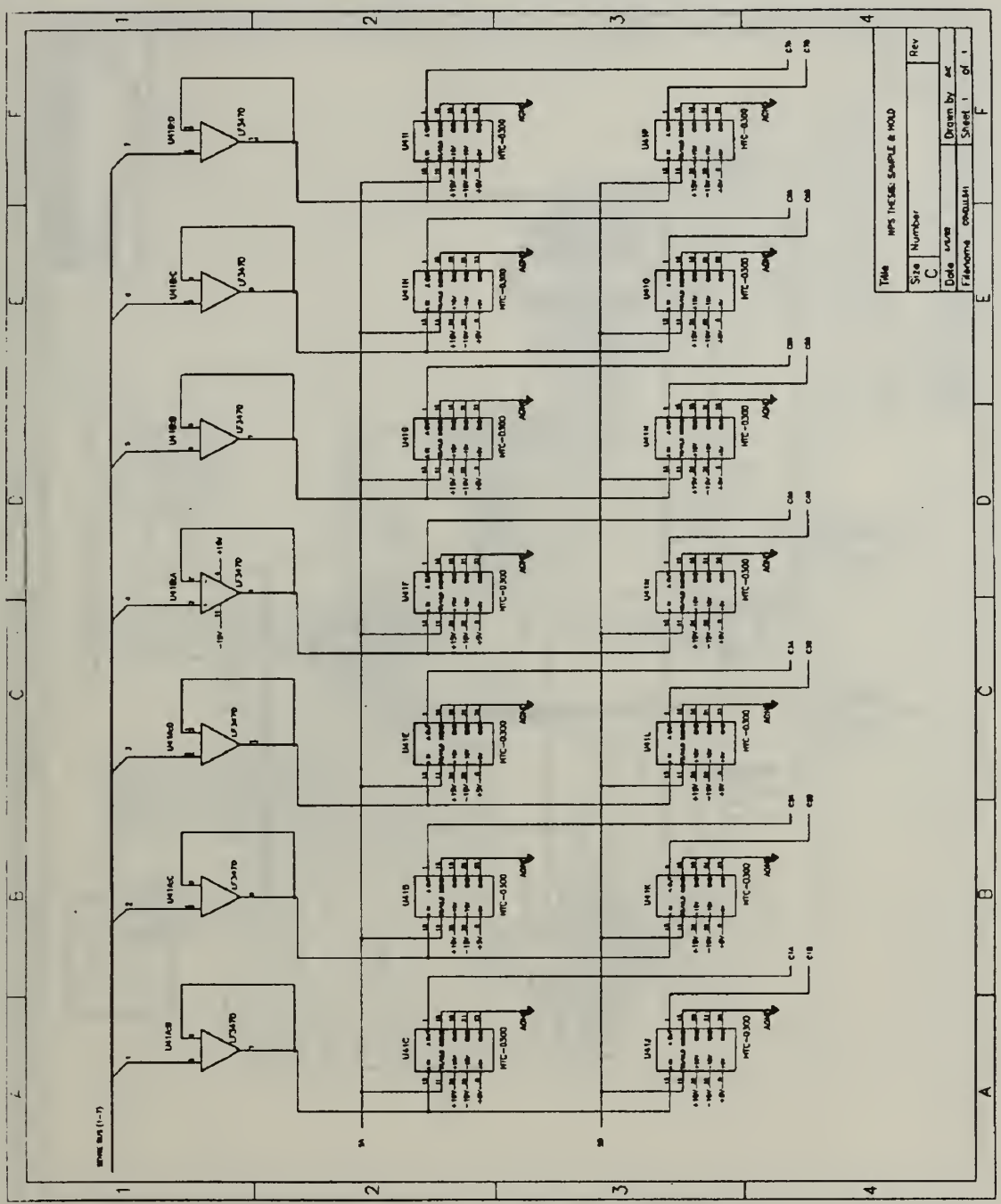
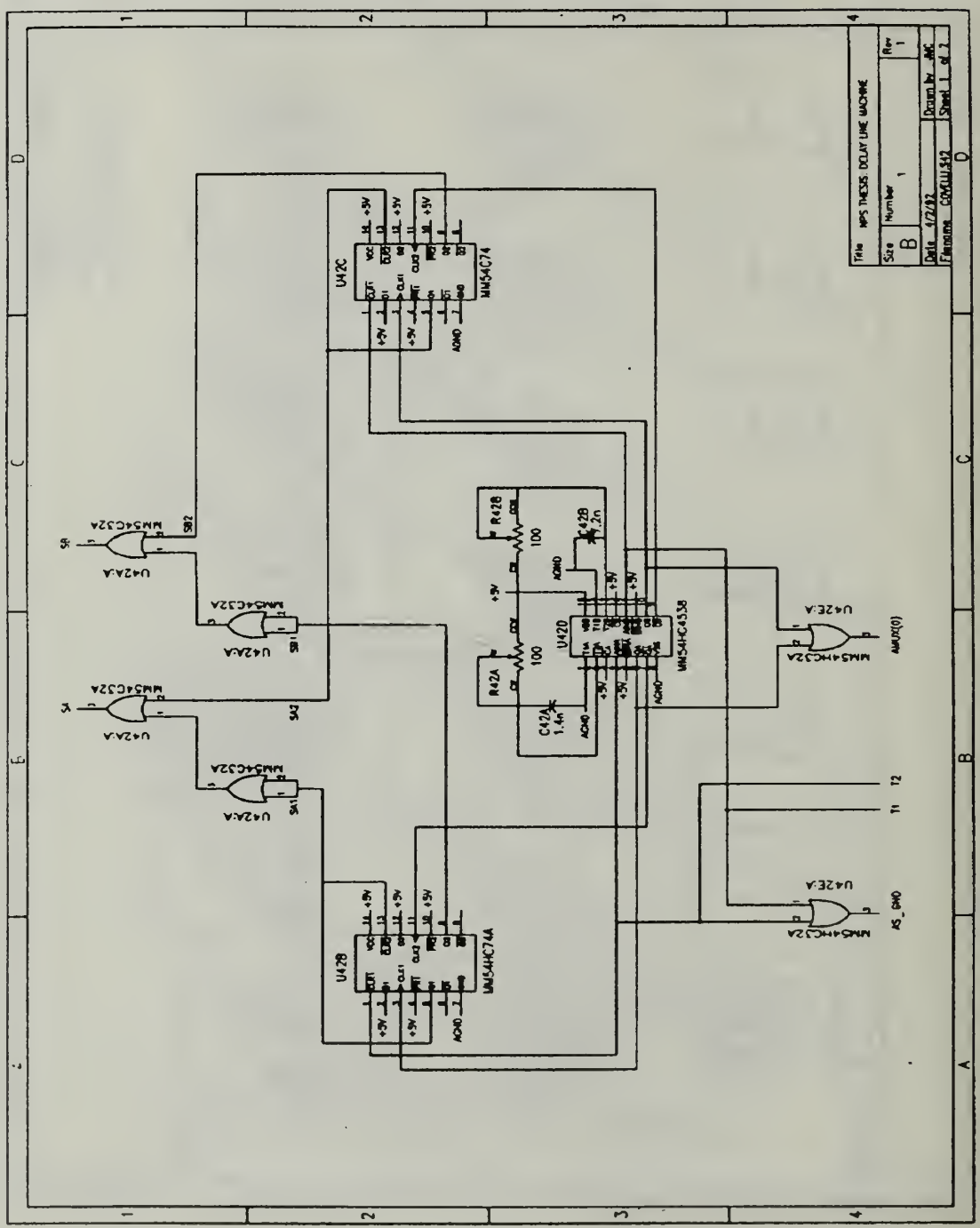
A/D_CONV
U40F
AD574
U40E-A
LF347D
R40A
R40B
100
VREF
AGND
U40D
AD7506
SAMPLE
&
HOLD
DELAY
LINE
MACHINE
U40A
U40B
U40C
LF13201
SENSE BUS (1-7)
CONTROL BUS (1-28)
ANALOG SWITCH I/O CHO
Title NPS THESIS: DATA COLLECTION
Size B
Number 1
Rev 1
Date 4/2/92
Drawn by AMC
Filename COVELLI.S40
Sheet 1 of 2

NPS THESIS: SAMPLE & HOLD (COVELLI.S41)

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Rev 1
Date 4/2/92
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Sheet 1 of 1
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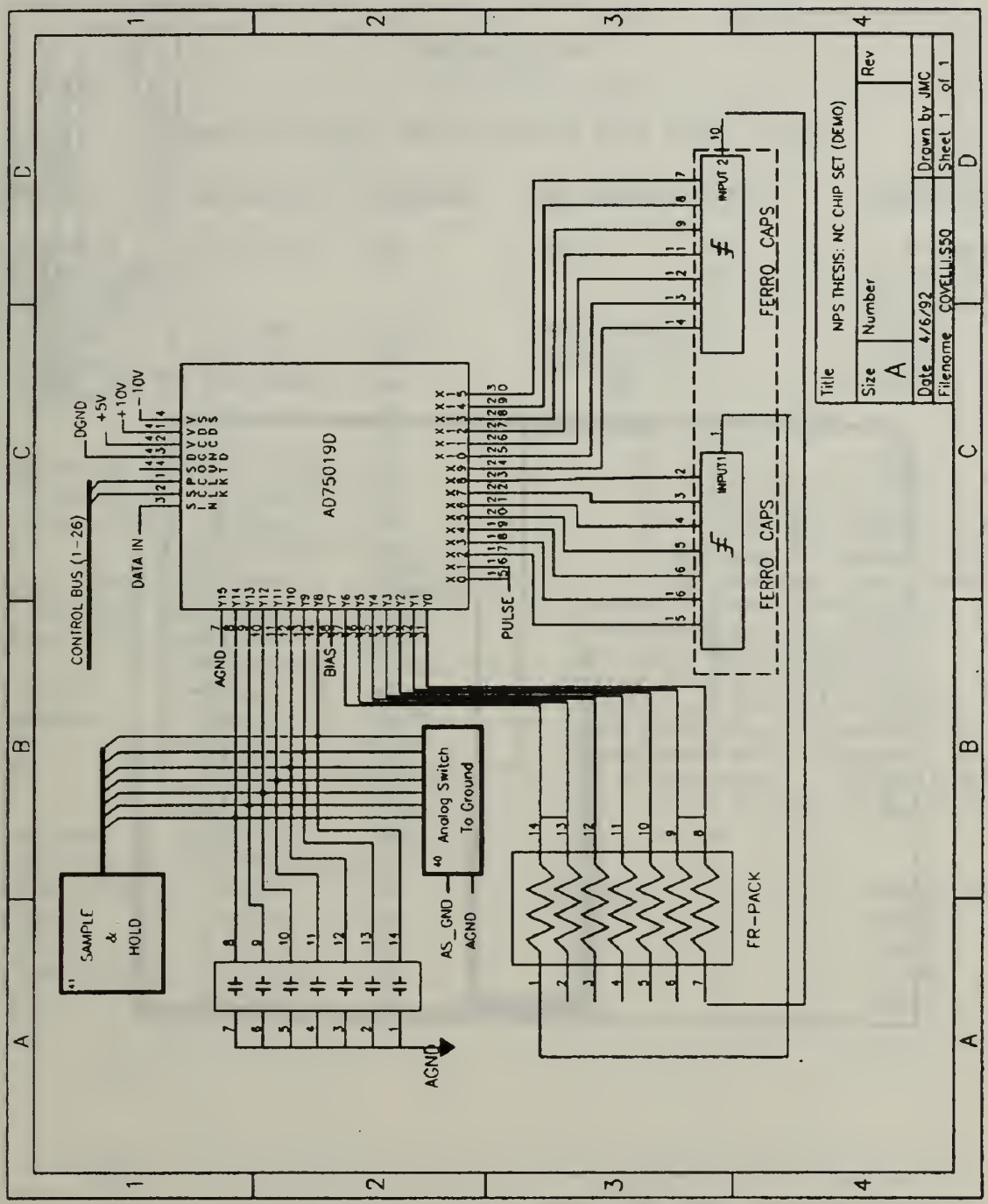
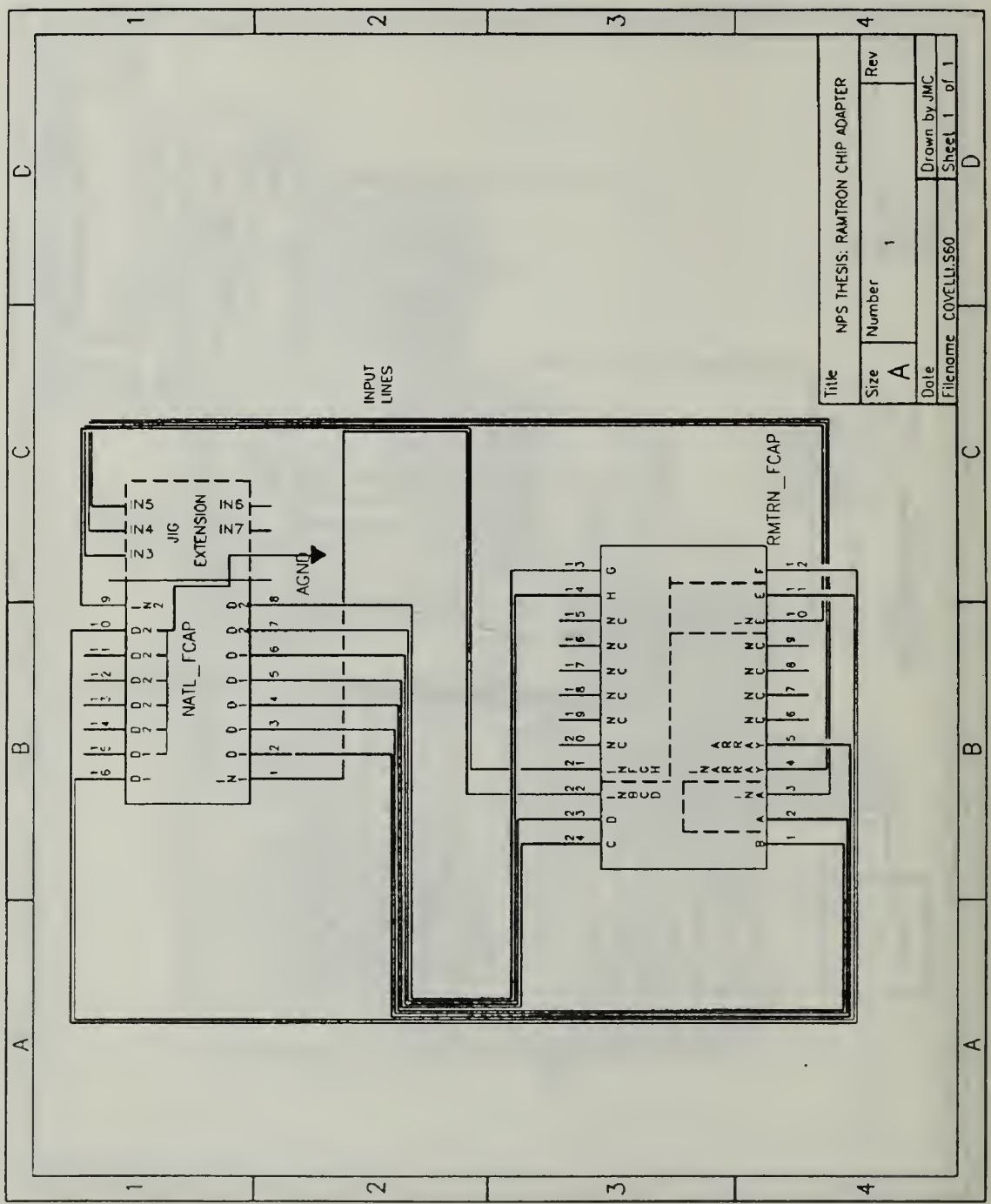
MM54C74
U42A:A
MM54C32A
U42B
MM54HC74A
U42D
MM54HC4538
U42E:A
MM54HC32A
R42B
100
C42B
4.2n
R42A
100
C42A
1.4n
AGND
+5V
SR2
SR1
SR3
AMUX(0)
AS_GND
T1
T2

NPS THESIS: NC CHIP SET (DEMO) (COVELLI.S50)



NPS THESIS: RAMTRON CHIP ADAPTER (COVELLI.S60)



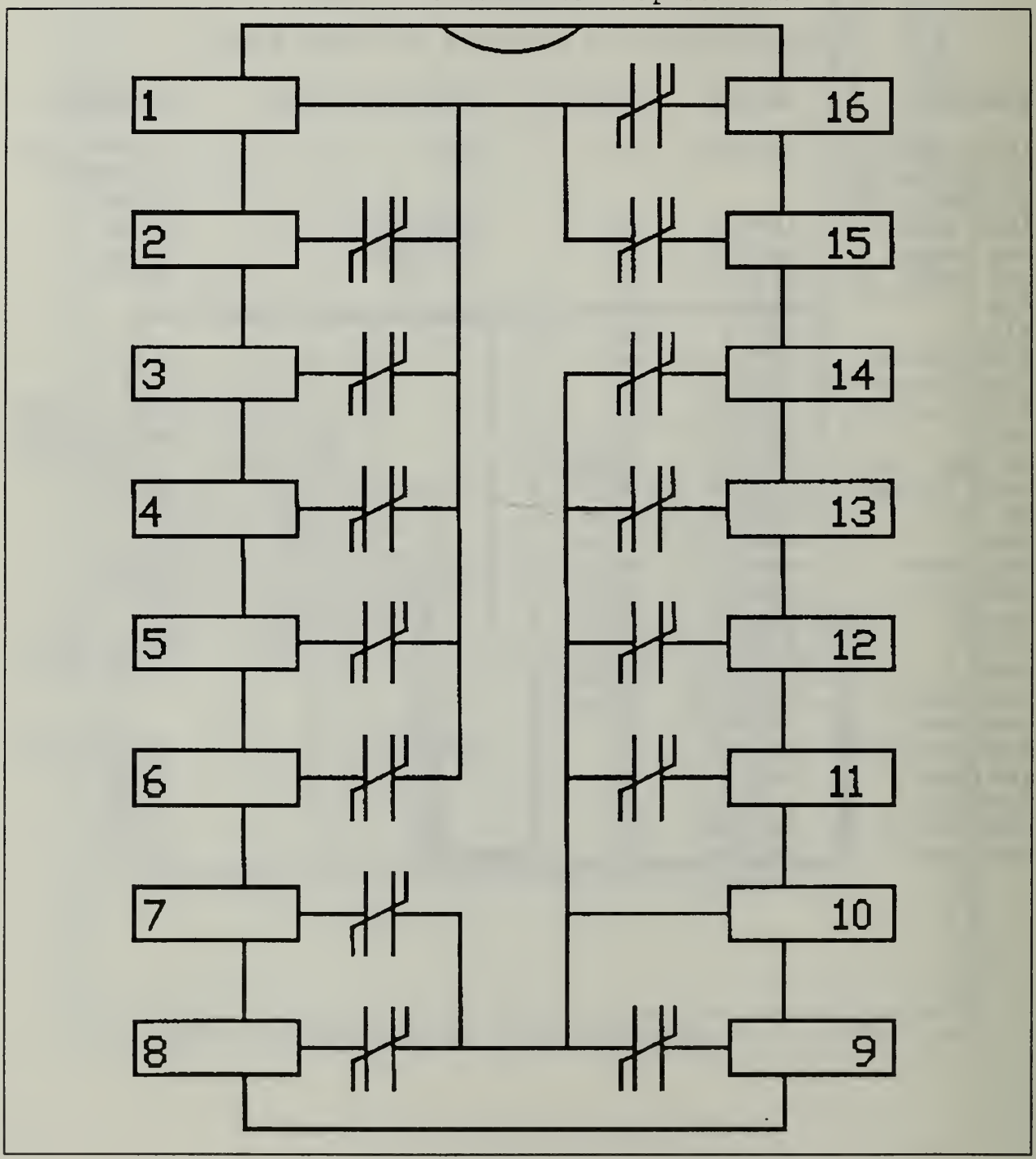
APPENDIX B

Itemized List of Hardware per Test Board

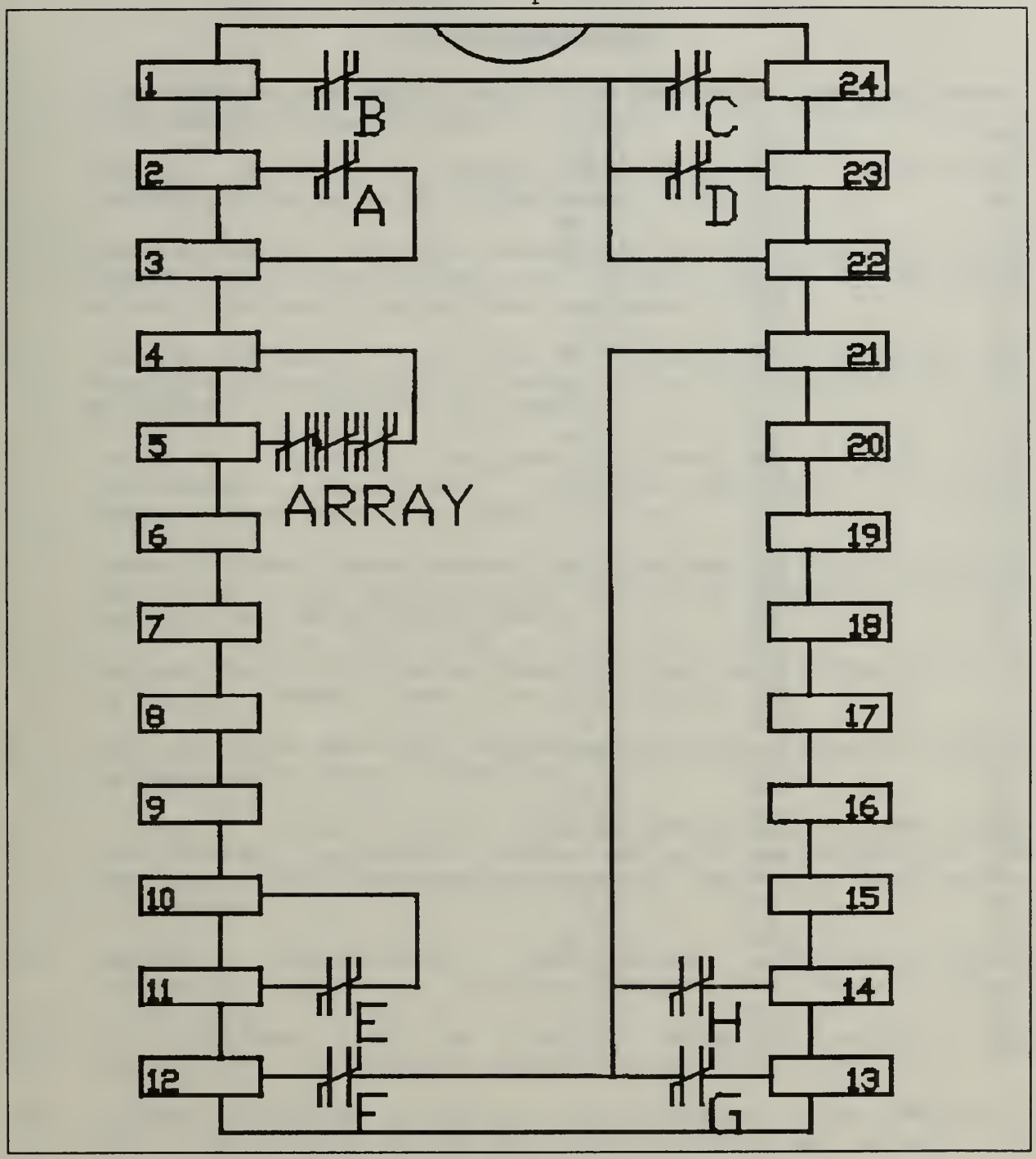
Function	Part #	Mnfctr	NS Equiv.	Qty	Comments
16x16 Amux	AD75019	AD	none	8	2 free ES
44-pin mount				8	1 Marvac
ZIF(24-pin)				8	wide
16x1 Amux	AD7506	AD	2xCD4051	1	slow
8x1 Amux	AD7501	AD	CD4051BM	1	slow
8x1 Amux	54HC4051	NS		4	fast
D/A	DAC1232	NS		1	
A/D	AD574	AD		1	
Track&Hold	HTS0300	AD		14	fast
8-bit Counter	54LS469	NS		6	
Function Gen.	LM566C	NS		1	10k-474kHz
(VCO	*74S624*	*TI*		*1*	*100k-10MHz)*
Op Amp (fast)	HA2540	Harris		1	4 free ES
Buff Op Amp	LF347D	NS		3	quad
An comp	54C909	NS		1	
PAL	PAL16L8			1	
Registers	74HCT573	NS	74C374	2	octal
Transever	CD4016	NS		2	quad
JK-ff	54HC73	NS		2	
D-ff	54C74	NS		1	dual,slow
D-ff	54HC74	NS		1	dual,fast
Tri-state	54C244A	NS		4	
One-shot	54HC4538	NS		1	
Aswitch(JFET)	CD4066	NS	LF13201	2	fast(60ns)
INV(hex)	54C04	NS		1	slow
INV(hex)	54HC04	NS		1	fast
NOR,INV (2,1)	CD4000M	NS		1	slow
OR(quad)	54C32A	NS		2	fast

APPENDIX C

National Semiconductor Chip Pin-out



Ramtron Chip Pin-out



APPENDIX D

Machine Language Program "TEST.COM" writen with IBM Dos 3.3 DEBUG

```
100             MOV         DX,303
103             MOV         AL,80
105             OUT         DX,AL
106             MOV         CX,100
109             MOV         DX,302
10C             MOV         AL,01
10E             CMP         CX,01
111             JNZ         116
113             OUT         DX,AL
114             JMP         139
116             CMP         CX,121
119             JNZ         11E
11B             OUT         DX,AL
11C             JMP         139
11E             CMP         CX,30
121             JNZ         126
123             OUT         DX,AL
124             JMP         139
126             CMP         CX,40
129             JNZ         12E
12B             OUT         DX,AL
12C             JMP         139
12E             CMP         CX,50
131             JNZ         136
133             OUT         DX,AL
134             JMP         139
136             MOV         AL,0
138             OUT         DX,AL
139             MOV         DX,300
13C             MOV         AL,1
13E             OUT         DX,AL
13F             MOV         AL,0
141             OUT         DX,AL
142             DEC         CX
143             MOV         DX,302
146             OUT         DX,AL
147             JG          10C
149             MOV         DX,300
14C             MOV         AL,2
14E             OUT         DX,AL
14F             MOV         AL,0
151             OUT         DX,AL
152             RET
```

LIST OF REFERENCES

1. Alan Clements, *Microprocessor System Design,* pp. 214 & 276, PWS Computer Science, Boston, 1987.

2. Michael Bloom, "A Memory to Remember," *Nonvolatile Semiconductor Memories,* IEEE Press, 1989.

3. Randy L. Wight, *Radiation Damage and Fatigue Breakdown in PZT Ferroelectric Capacitors,* M.S. Thesis, Naval Postgraduate School, Monterey, California, December 1990.

4. Carl E. Josefson, *Evaluation of Ferroelectric Materials for Memory Applications,* M.S. Thesis, Naval Postgraduate School, Monterey, California, June 1990.

5. Steve E. Bernacki, "Raytheon Ferroelectric Thin Film Development Consortium," Raytheon Equipment Division, Sudbury, Massachusetts, 1989.

6. Robert Newham, "Basic Properties of Ferroelectric Materials," presented at the Ferroelectric Materials Tutorial, Colorado Springs, CO, 28-29 March 1989.

7. Bernard Jaffe, William R. Cooke and Hans Jaffe, *Piezoelectric Ceramics,* Academic Press, New York, 1971.

8. IEEE Standard 180-1986, IEEE Standard Definitions of Primary Ferroelectric Terms, June 1986.

9. B. Hestir, "User's Guide to the Stress and Measurement (SMS) Test System," Appendix C, submitted as a design project for ECE 2990, Naval Postgraduate School, Monterey, California, Fall 1989.

10. Ramtron International Corporation, *Ferroelectronics Technology Background,* Colorado Springs, CO, January 1991.

11. J.C. Burfoot and G.W. Taylor, *Polar Dielectrics and Applications*, University of California Press, 1979.

12. Laureen H. Parker and Al F. Tauch, "Ferroelectric Materials for 64 Mb and 256 Mb DRAMs," *IEEE Circuits and Devices*, v. pp. 17-26, January 1990.

13. Joe Evans et al., "A Ferroelectric NDRO Memory Device," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

14. Yoichi Miyasaka et al., "High Dielectric Constant (Ba,Sr)TiO_3 Thin Film for DRAM Capacitor Application," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

15. Takashi Mihara, C.A. Paz de Araujo et al., "Memory Device Feasibility and Electrical Characterization of a Newly Developed Fatigue-Free Ferroelectric Capacitor," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

16. B.M. Melnick, C.A. Paz de Araujo et al., "Anomalous Fatigue-Free Behavior in Zn Doped PZT," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

17. J.R. Schwank et al., "Total-Dose Radiation-Induced Degradation of Thin Film Ferroelectric Capacitors," *IEEE Transactions on Nuclear Science*, v.37, pp. 1703-1712, December 1990.

18. J.M. Benedetto et al., "The Effect of Ionizing Radiation on Sol-Gel Ferroelectric PZT Capacitors," *IEEE Transactions on Nuclear Science*, v.37, pp. 1713-1717, December 1990.

19. S.L. Miller and P.J. McWhorter, "Device Physics of the Ferroelectric Memory Field Effect Transistor," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

20. L.T. Clark et al., "Measurement and Simulation of Partial Switching in Ferroelectric PZT Thin-Films," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

21. Maseo Takahashi, "Space Charge Effect in Lead Zirconate Titanate Ceramics caused by the Addition of Impurities," *Japanese Journal of Physics*, v.9, pp. 1236-1246, October 1970.

22. Naval Research Laboratory Report 7172, *Aging of Barium Titanate and Lead Zirconate-Titanate Ferroelectric Ceramics*, by Jules DeLauney and Paul L. Smith, 15 October 1970.

23. J.F. Scott and B. Pouligny, "Raman Spectroscopy of Submicron KNO_3 films. II. Fatigue and Space-charge Effects," *Journal of Applied Physics*, v.64, pp. 1547-1551, 1 August 1988.

24. W.R. Salaneck, "Some Fatiguing Effects in 8/65/36 PLZT Fine Grained Ferroelectric Ceramic," *Ferroelectrics*, v.4, pp. 97-101, 1972.

25. J.F. Scott and P.A. Paz de Araujo, "Ferroelectric Memories," *Science*, v.246, pp. 1400-1405, 1989.

26. John Free, "Electronic Newsfront: FCLD panels," *Popular Science*, p. 36, May 1992.

27. S.H. Lee et al., "Ferroelectronic Thin Films in Optoelectronic Computing Systems," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

28. P. Shiller et al., "Design and Process Considerations for Ferroelectric Film-based Piezoelectric Pressure Microsensors," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

29. J.F. Scott and T. Chen, "A PMN Photonic Sensor," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

30. K. Takenaka, W. Larson et al., "A 1T/1C 256K Non-Volatile Ferroelectric Memory," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

31. Nicholas M. Shorrocks and Ivan M. Edwards, "Design and Performance of Thermal Imaging Arrays," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 58-62, 1990.

32. Wallace A. Smith, "The Application of 1-3 Piezocomposites in Acoustic Transducers," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 145-152, 1990.

33. Akio Kumada, "Piezoelectric Revolving Motors Applicable for Future Purposes," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 213-219, 1990.

34. Kiyoshi Yoda et al., "Impact Printer Head using Piezoelectric Actuators," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 225-228, 1990.

35. Ki-Young Oh et al., "Development and Application of Shape Memory Ceramic Actuators," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 525-527, 1990.

36. Atsushi Furuta et al., "Mechanical Clamper using Shape Memory Ceramics," *IEEE 7th International Symposium on Applications of Ferroelectrics*, pp. 528-529, 1990.

37. Letter from Norman Abt, National Semiconductor, Santa Clara, California, 7 November, 1991.

38. Letter from William A. Geideman, McDonnell-Douglas Electronic Systems Company, Santa Ana, California, 22 November, 1991.

39. Radiant Technologies Inc., *RT66A Operating Manual,* Albuquerque, NM, October 1991.

40. W.R. Hestir, *Automated Testing of On-chip Ferroelectric Capacitors,* M.S. Thesis, Naval Postgraduate School, Monterey, California, December 1990.

41. T. Gloerstad et al., "Dynamic Characterization of Dielectric Thin-Films," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

42. R.D. Nasby and M.S. Rodgers, "Fatigue and Testing of Thin-Film Ferroelectric Capacitors," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

43. Orbital Science Corporation, *Advanced Photovoltaic and Electronics Experiment (APEX) Mission, Preliminary Mission Operations Requirements Definition and Preliminary Spacecraft Design Requirements and Approach,* technical report, 1990.

44. Steve Bernacki, Standardized Ferroelectric Capacitor Testing Methodology For Nonvolatile Semiconductor Memory Applications," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

45. N. Abt et al., "High Frequency Fatiguing of Ferroelectric Capacitors," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

46. Conversation with Norman Abt, National Semiconductor, Santa Clara, California, 11 March, 1992.

47. J. Evans, M. Ivey and J. Bullington, "Testing for Fatigue and Aging in Ferroelectric Thin-film Capacitors," *First Symposium on Integrated Ferroelectrics*, pp. 217-221, March 1989.

48. H. Watanabe, T. Mihara and H. Yoshimori, "Fatigue Properties of PZT Thin Films Prepared by Sol-Gel Methods," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

49. M. Lakata, S. Thakoor and S. Bernacki, "Pulse Testing of PZT Ferroelectric Memory Capacitors for Space Applications," presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

50. S. Bernacki, Raytheon Equipment Division, U.S. Army SDC minutes, presented at the 4th International Symposium on Integrated Ferroelectrics, Monterey, California, March 1992.

51. Analog Device AD75019 specifications and errata, FAXed on 10 October, 1991.

52. National Semiconductor, *CMOS Data Book*, 1981.

53. National Semiconductor, *CMOS Logic Data Book*, Rev. 1, 1988.

54. Harris Corporation, *Digital Product Data Book, Military,* Woburn, Massachussetts, 1989.

55. Analog Device, *CMOS Product Data Book*, 1987.

56. Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, pp. 263-267, Holt, Rinehart and Winston Inc., New York, 1987.

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